doi:10.1017/S1431927613008428
Microsc. Microanal. 19 (Suppl 2), 2013
© Microscopy Society of America 2013

Quantitative Energy Dispersive Analysis Technique of SiGe at Site-Specific Area using In-Situ Lift-Out TEM Sample

Tae-Su Park, Hyo-Jin Kang, Jie-Won Chung, Byoung-Muk Song, Tae-Sun Back, Ho-Joung Kim, and Chang-Reol Kim

Research And Development Division, SKhynix Semiconductor Inc., San 136-1, Ami-ri, Bubal-eub, Ichon-si, Kyoungki-do 467-701, Korea

Lately as the semiconductor design rule got smaller, there emerged the need to secure enough drive current for transistor. So we were determined to improve mobility by using SiGe epitaxial layer which is superior in mobility to conventional Si substrate. SiGe is commonly used as a semiconductor material for hetero junction transistors or as a strain-inducing layer for transistors. In order to use this SiGe layer architecture in semiconductor devices, we needed quantitative analysis of patterned wafer including SiGe. For patterned wafer analysis of a feature size smaller than 0.1 um in size, scanning transmission electron microscope (STEM) equipped with energy dispersive spectroscopy (EDS) could be very useful method for quantitative analysis. A reference sample with known composition is also required for meaningful quantitative analysis. So we have obtained quantitative data of reference sample for SiGe in non-patterned wafer by auger electron spectroscopy (AES). We executed EDS analysis on same sample and secured conditions for quantitative analysis. TEM sample have been prepared by focused ion beam (FIB) systems in order to prepare site-specific sample in patterned wafer. Quantitative analysis of experiments was performed by Hitachi HD2700 dedicated STEM. During this process, we verified many artifacts that can occur from EDS analysis, and figured out that not only analysis conditions but also sample preparation conditions are important factor of EDS quantitative analysis. In- situ lift-out (INLO) TEM sample preparation was more effective method for quantitative analysis than ex-situ lift-out (EXLO) method.

As a result, we made it possible to do quantitative analysis of SiGe epitaxial layer by EDS in patterned wafer, and formed the basis to analysis about the relationship between electrical characteristic of devices and quantitative analysis of SiGe composition.

References:

[1] Wen-Shiang Liao *et al*, IEEE ELECTRON DEVICE LETTERS, Vol. 29 (2008) p. 86.
[2] L. GARCHERY *et al*, Mat. Res. Soc. Symp. Proc.Vol. 379 (1995) p. 333.
[3] A.Hikavyy *et al*, ECS Transactions, Vol. 25 (2009) p201.
[4] Chung-Uao Fu *et al*, Solid-State Electronics 53 (2009) p. 888.

https://doi.org/10.1017/S1431927613008428 Published online by Cambridge University Press

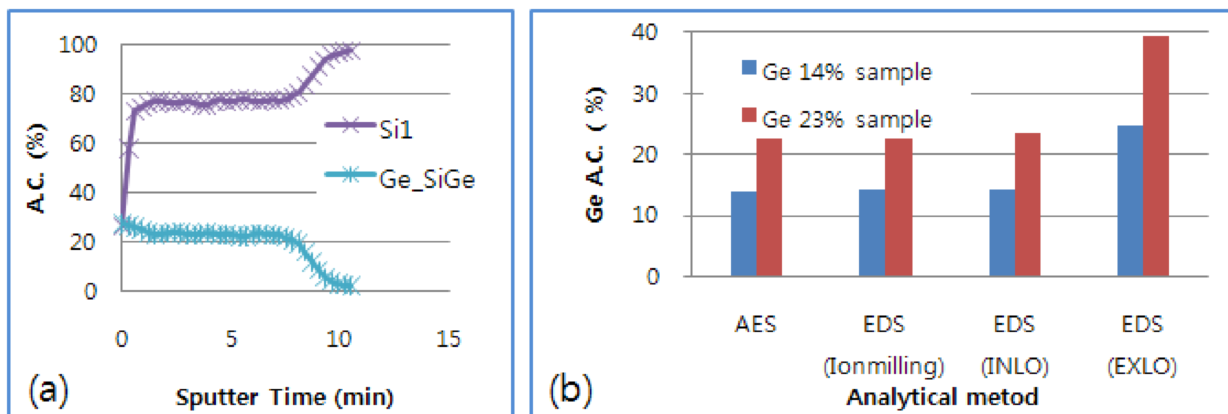

Figure 1. AES profile of Ge and Si (a), Ge contents as measure with AES and EDS (b) from SiGe structure in non-patterned wafer

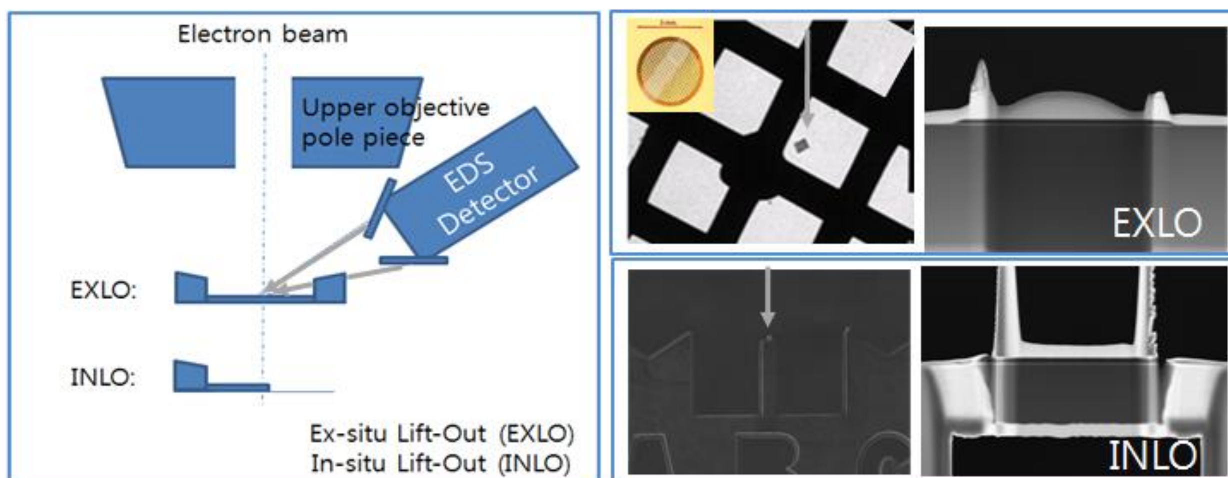

Figure 2. Geometry of TEM sample by EXLO and INLO method for quantitative analysis

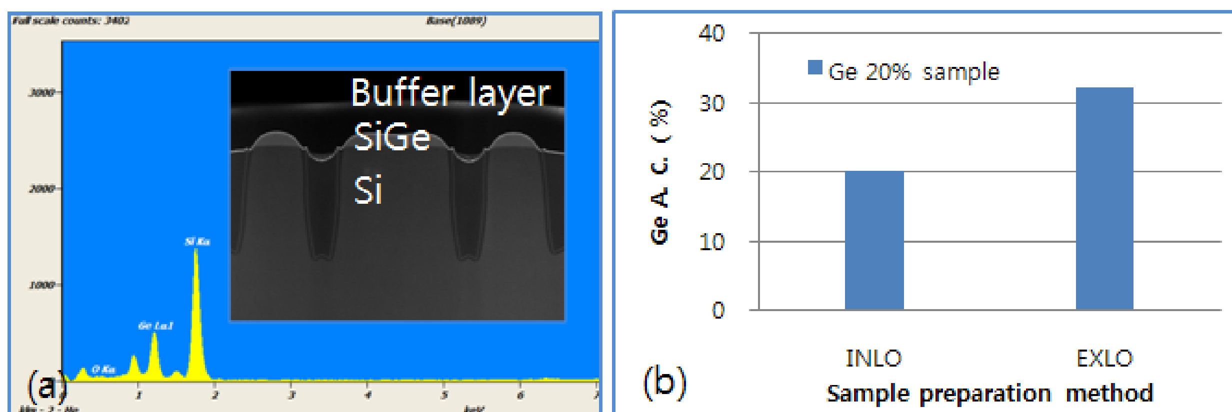

Figure 3. Spectrum and STEM image (a), Ge contents with EDS (b) of SiGe in patterned wafer

https://doi.org/10.1017/S1431927613008428 Published online by Cambridge University Press