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Xe Plasma vs Gallium FIB Delayering

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Layer-by-layer deprocessing is becoming increasingly vital and challenging for industrial and research applications such as failure analysis, chip reverse engineering, and patent violation detection. Ga focused ion beam (FIB) and Xe FIB instruments are the go-to tools for chip material analysis in the semiconductor industry for applications like TEM lamella preparation, circuit edit, and cross-sectional analysis. A common technique for delayering has been mechanical polishing which is not precise or localized enough in removing sensitive layers on IC chips [1,3]. We have previously used a Xe FIB successfully for delayering on sub-14 nm technology from metal 8 to transistor contacts in combination with special gas chemistry [4]. Here we show that a Ga FIB with the same chemistry as the Xe FIB can also perform delayering on sub 14 nm technology microprocessor and we will discuss the differences between the two use cases.

Top-down delayering of sub-14 nm technology nodes were performed with both Ga and Xe FIBs using A-Maze special gas precursor (proprietary and patented gas chemistry of TESCAN ORSAY Holding a.s.). Figure 1a shows a 100 x 100 µm² area opened on sub-14 nm using Xe FIB by aligning the sample analytical working distance to the SEM positioned orthogonal to the FIB beam. A GIS was inserted to inject A-Maze gas onto the area of interest. Suitable current density and beam shape was used to conduce planarity in the presence of the gas chemistry and the process was monitored using end point detection based on the SE signal being generated during the etching process (Figure 3). The end pointing recognizes peaks as the metal layer and troughs as the via layer which gives full control to the operator to start and stop the process in any layer of interest. Fine polishing is performed once a specific layer is reached to get rid of residual metal/dielectric from the previous layer removed. Figure 2a shows 20 x 20 µm² block of area opened using Ga FIB and Figure 2b shows the details of via contacts uncovered illustrating final planarity and accessibility to the layer architecture for pattern recognition and detecting spyware circuitry.

In this paper, the extended capability of a Ga FIB with special gas chemistry is demonstrated by performing delayering on an Intel 14 nm chip. Ga FIB or Xe FIB with A-Maze or Nanoflat gas based assisted etching (FIB-GAE) can remove dissimilar materials with similar removal rates producing final roughness of the exposed area under 10 nm RMS for the overall topography. The method delivers significant advantages in terms of localized, precise and layer-by-layer removal along with constant monitoring using the acquired SE signal for end point detection. The process is capable of performing delayering for 10-12 layers on sub-20 nm process nodes. The usual size of the area exposed with delayering can be as big as 20 µm and can be achieved in about 12 minutes. It enhances the workflow capability by enabling yet another application for a Ga FIB and making a 'must-have' tool in semiconductor for physical failure analysis as well as cyber-security applications.

Gallium implantation in exposed layers is a known drawback which hinders most electrical characterization techniques. This is where Xe FIB can be of assistance and can help prepare larger delayered areas (M8 to TCL, size up to 200 µm edge length in under 30 minutes) offering access to a wider range of area to perform nanoprobing (Figure 1b) and TEM lamella preparation for further analysis.

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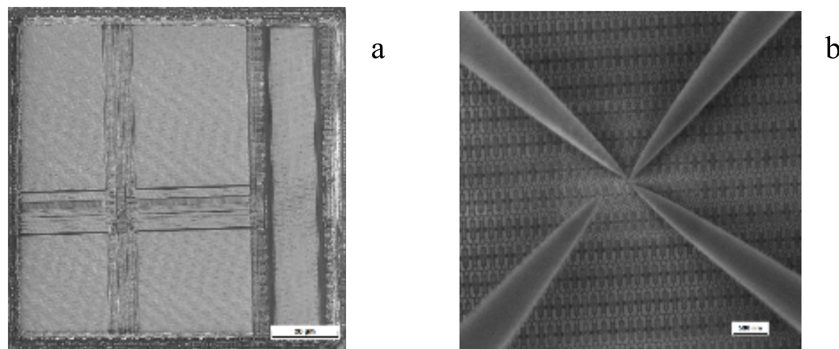

Figure 1. (a) Delayered window with Xe FIB to transistor contacts. (b) Nanoprobes performing electrical measurement on a PMOS.

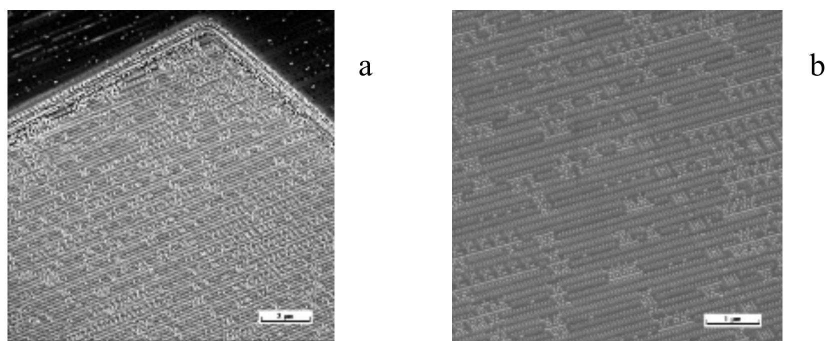

Figure 2a and 2b. Delayered box of 20x20 µm² with smooth walls.

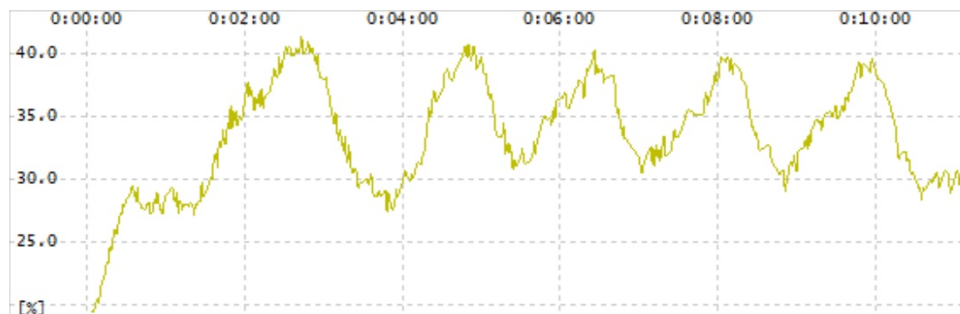

Figure 3. Typical end point detection (EPD) generated to help monitor and control layer removal – each peak is a metal layer and trough is recognized as via layer.

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