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Developing High Resolution and High Precision Strain Mapping Methodologies for Materials Research and Semiconductor Technology

Jian-Min Zuo[1,2], Renliang Yuan[1,2], Honggyu Kim[1,2] and Jiong Zhang[3]

[1]Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA
[2]Fredrick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA
[3]Intel Corp., Hillsboro, Oregon, USA

Strain and the related stress in nanoelectronic devices play a critical role in semiconductor technologies. In general, strain arises from the lattice mismatch between dissimilar materials and thus strain is critical for the design and growth of epitaxial heterostructures in micro- and nano-electronics. In transistors, strained silicon channels provide a major boost to the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs), e.g., the use of epitaxial strain of Si and Ge alloys in PMOS [1]. In the near term, the transistor technology is pushing towards the sub 10 nm technology node. At this length scale, resolving strain in the devices requires a resolution of sub nanometer with not only high resolution, also high accuracy and reliability. The use of novel architectures and alternative materials in the transistor technology also demands metrology capable of handling these structural and material changes.

High resolution strain measurement can be performed using high energy electrons either in reciprocal space using transmission electron diffraction (TED) [2], or scanning precession electron diffraction (SPED) or in real space through direct imaging using high resolution electron microscopy (HREM), scanning transmission electron microscopy (STEM) [3] or dark-field electron holography (DFEH) [4]. The resolution and strain measurement sensitivities range from Å to several nm and 10^{-3} to 10^{-4} respectively. Recent developments in aberration corrected STEM especially have improved the spatial resolution to sub-Å and the precision of measuring atomic column positions to picometers [3].

TED in the form of scanning electron nanodiffraction (SEND) or nanobeam electron diffraction (NBED) has been widely used to characterize nanocrystalline materials due to its high sensitivity to local structure and ability to focus electron beam to nm or sub-nm size. By controlling the built-in (S)TEM deflection coils, we can scan the nano-beam across desired sample area and acquire a series of diffraction patterns over a region of interest [5]. This technique is most versatile for strain mapping across difference length scales from sub-nm to micron. However, data processing and data interpretation present significant challenges for TED. A dataset for 2D-SEND scan easily contains thousands or more diffraction patterns that requires a fast and robust algorithm to identify the diffraction peak positions. In strained nanostructure, the intensity and position of diffraction peaks depend sensitively on beam convergence angle, electron multiple scattering and sample.

This talk will first review high resolution and high sensitivity electron beam techniques for strain characterization in nanodevices and device materials. Examples include planar and a finfet transistors and III-V heterostructures [6,7]. We then propose new SEND approaches and algorithms for high resolution and high sensitivity strain mapping, which will be demonstrated using a combination of experimental data and multislice simulations [8].

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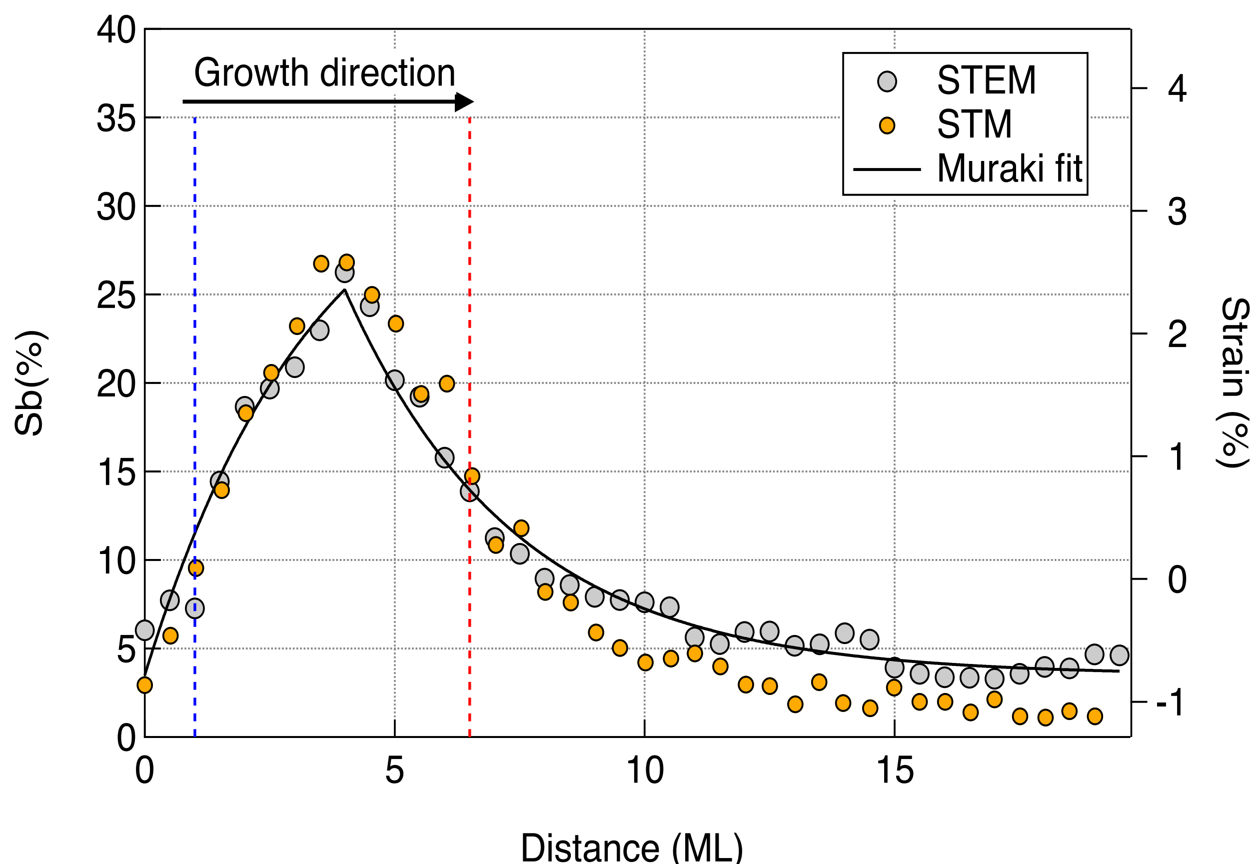

Figure 1. Atomic resolution strain mapping using STEM in an InAs/InAsSb superlattice. (a) Strain map along x (horizontal) obtained using template matching. (b) calculated strain based on the average Sb composition in (d). (c) Difference between experimental strain and computed strain maps, showing deviations from the average strain. (e) A plot shows the correlation between strain fluctuations and Sb composition (data from [7]).

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