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Measurement of LER in Poly-Silicon gates in MOSFETS by (S)TEM

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A key parameter controlling the performance of MOSFET devices is the channel length or poly-silicon gate width sometimes known as L_{poly}. As devices scale smaller and the L_{poly} shrinks, the effect of variations of L_{poly} over the length of the device is seen to have increasingly more pronounced effects on critical device characteristics such as threshold voltage, and device off currents [1,2]. Figure 1 is a plan-view schematic depicting the L_{poly} gate-length variations across the length of the active device area. The International Technology Roadmap for Semiconductors (ITRS) [3] lays out targets for crucial device parameters, one of which is the limit on the L_{poly} Line Edge Roughness (LER). According to the roadmap, by 2010 the 45nm technology node will have L_{poly} lengths down to 18nm and critical dimension control will need to be better than 1.3nm. This paper addresses a method used to measure LER and not the processing conditions contributing to it.

The widespread method used to determine LER is in-line SEM. A key drawback to this approach is that the lines are inspected early in the process line, either during lithography or immediately after etching. Subsequent processing steps to the Si involve thermal anneals, ion-implants, oxidation steps, silicidation which can modify the LER. To monitor L_{poly} after these processes it is common to prepare cross-sectional samples, followed by TEM. To provide a reliable estimate of the average L poly, multiple gates need to be sectioned and little or no insight is gained on the LER, especially since cross section TEM is a projection through the sample thickness which often is 100nm. By performing a plan view inspection the poly lines can be observed directly at comparable resolution. In this study we have used plan view TEM to inspect the L_{poly} lines up to 2um in length with 1-2nm spacing, by recording and splicing several line segments together.

Chips are delayered by mechanical polishing into the gate structure. Since the L poly dimension closest to the underlying doped Si RX region is most critical it is important to ensure the delayering is achieved to within 50 nm of the RX. An electron transparent sample can then be prepared by backside grinding, dimple and etching, ion-milling or FIB. Imaging has been carried out in bright field TEM mode, BF STEM mode using a large illumination angle to minimize phase contrast and diffraction effects and High angle ADF stem. Examples are shown in figure 2 and 3. After acquisition, data are imported into SIS software and processed using the line-width toolbox. The outputted L_{poly} values are loaded into MATLAB to carry out a power spectrum analysis. The LER is defined as the standard deviation of the L_{poly} measurements shown in figure 4. It is commonly found that no systematic dependence of the LER on sampling period. The variance of the mean LER is reduced significantly with increased sampling points. In the example shown, the power-spectrum of the L_{poly} measurements shows that for the line examined there is no dominant frequency contributing to the LER. In general it is found that the high frequency cut-off is aligned to the mean grain size of the poly and the normalized cumulative sum indicates that 90% of the variability in the LER occurs over length scales exceeding 10nm. Effects such as grain boundary grooving often seen in the images do not appear to significantly contribute to the LER.

References

[1] Linton et al., IEES Silicon Nanoelectronics Workshop, 1999, pp28-29
[2] Kane et al., ISFA 2004, 30th International Symposium for Testing and Failure Analysis

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[3] ITRS Roadmap, http://www.itrs.net/Common/2004Update/2004_13_Metrology.pdf

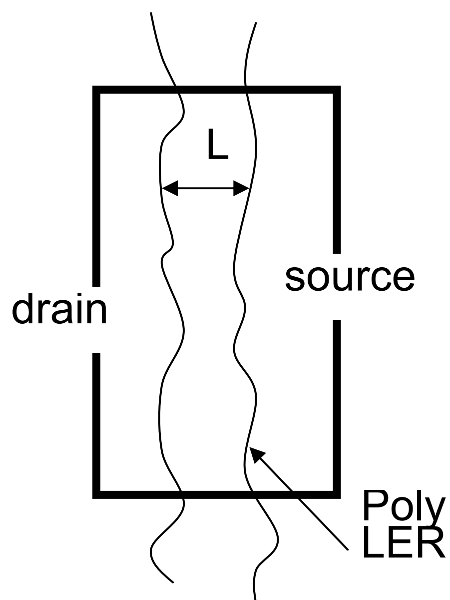

Figure 1: Schematic of LER for MOSFET device

Figure 2: Plan view TEM of poly gate structure

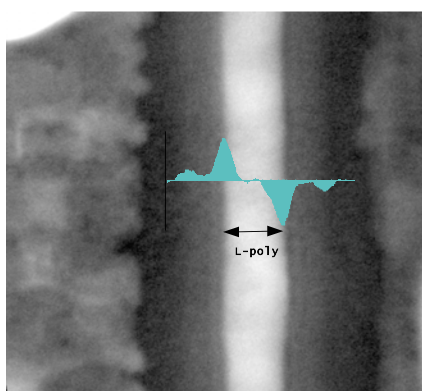

Figure 3: ADF stem image and 1st difference profile

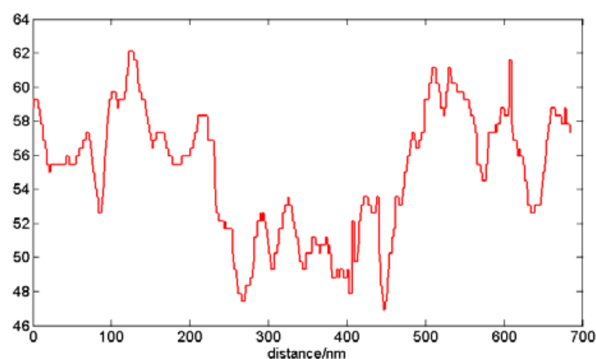

Figure 4: Line width measurements from STEM images

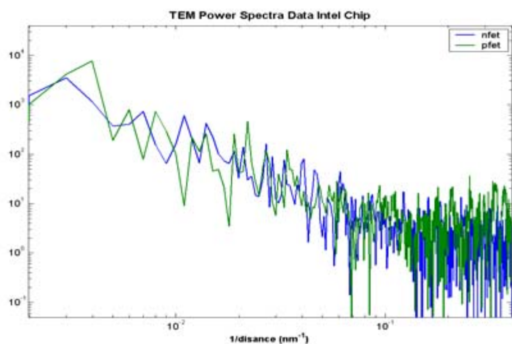

Figure 5: Power spectrum of LER data:

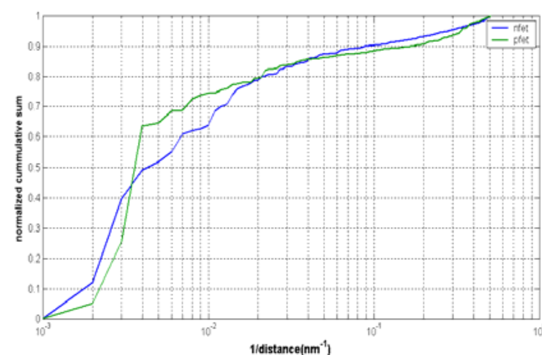

Figure 6: Cumulative sum plot