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ATOMIC LAYER DEPOSITION FOR EMERGING THIN-FILM MATERIALS AND APPLICATIONS

FOCUS ISSUE

Recent advances in the understanding of high-*k* dielectric materials deposited by atomic layer deposition for dynamic random-access memory capacitor applications

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Capacitors represent the largest obstacle to dynamic random-access memory (DRAM) technology evolution because the capacitor properties govern the overall operational characteristics of DRAM devices. Moreover, only the atomic layer deposition (ALD) technique is used for the dielectric and electrode because of its extreme geometry. Various high-*k* materials deposited by ALD have been investigated for further scaling. Whereas past investigations focused on increasing the physical thickness of the dielectric to suppress leakage current, the physical thickness of the dielectric should also be limited to a few nanometers in design rules less than 1×-nm. Therefore, a new way to overcome the limitations of traditional approaches based on thorough understanding of high-*k* materials is highly recommended to enhance the properties of conventional materials and provide directions for developing new materials. In this review, previously reported results are discussed, and suggestions are made for further investigations for DRAM capacitor applications.

Introduction

Dynamic random-access memory (DRAM) device is the most important device among semiconductor memory devices because of its wide range of applications in the IT industry, which include PCs, servers, and mobile phones. The necessity and importance of DRAM have increased because of the tremendous amount of data to be processed in the big data industry (which is one of the most important industries in the fourth industrial revolution) and the increased demand for various electronic devices [1]. In this regard, the market for DRAM has increased dramatically in the past decades, and this increase has reached unprecedented levels in recent years. As a consequence, research about DRAM devices has attracted a lot of attention from academia and industry. Because the capacitor primarily governs operational characteristics of the DRAM device, most research on DRAM has focused on implementing performance enhancements in the DRAM capacitor. The DRAM capacitor, which consists of a metal–insulator–metal (MIM) structure, requires low leakage current density and high capacitance density for robust operations (e.g., read, write, and refresh). In the early stages of development, decreasing the dielectric thickness or increasing the capacitance area by changing the structure of the MIM capacitor could be used to meet the specifications of DRAM capacitors [2, 3]. However, using dielectric materials with a high dielectric constant (*k*) was inevitable in the era of design rules beyond sub-100 nm [4, 5]. High-*k* materials allow the same capacitance density as a thicker physical thickness, which can effectively suppress the leakage current through tunneling mechanisms. However, additional problems have emerged when using high-*k* materials. First, other leakage conduction mechanisms offset the leakage current reduction effect observed when using the high-*k* dielectric [6, 7, 8, 9]. These mechanisms originate from large defect densities or narrow band gaps and include trap-assisted tunneling (TAT), Poole–Frenkel (P–F) emission, Schottky emission, or Fowler–Nordheim (F–N) tunneling. Moreover, further scaling beyond sub-10 nm causes new limitations in the physical thickness of dielectrics when designing MIM structures as thin as possible [4]. Ironically, the high-*k* material was originally introduced to realize a higher physical thickness [10]. As a consequence, the requirements of high-*k* materials for next-generation DRAM capacitor applications include both

conventional goals (e.g., low leakage current and high capacitance density) and the thinnest possible physical thickness.

Leakage current in the metal–insulator–metal structure with high-*k* materials

Leakage current through a dielectric layer in MIM capacitors results in severe degradation in DRAM device operation because data in a DRAM unit cell is stored by charging carriers in the MIM capacitor. In this regard, leakage current reduction is a key issue in DRAM device investigations, and this is the reason why high-*k* materials have been introduced as an insulator in the MIM capacitor. However, MIM capacitors with high-*k* materials have suffered from leakage currents because of the weak dielectric strength of high-*k* materials (Fig. 1) [11, 12]. Whereas direct tunneling should be considered as an only carrier conduction mechanism in the case of using SiO_2, several such mechanisms could contribute to leakage current when using high-*k* materials, resulting in weak dielectric strength of high-*k* materials. Figure 2 depicts the carrier conduction mechanisms available in ZrO_2 as an example of high-*k* materials [6]. As shown in Fig. 2, the carrier conduction mechanisms are related to defects (e.g., TAT and P–F emission) or low conduction band offsets (CBOs) (e.g., Schottky emission and F–N tunneling). In this regard, these mechanisms can be classified into two categories: bulk-related or interface-related leakage current conduction.

Bulk-related leakage current conduction

ZrO_2 and HfO_2 have been extensively studied as high-*k* materials for replacing classical SiO_2 and SiON insulators because of their relatively high *k* value (>20), wide band gap (E_g) of 5.5–6.0 eV, and well-established atomic layer deposition (ALD) processes [13, 14, 15, 16, 17, 18, 19, 20]. Although ZrO_2 and HfO_2 share many common properties, ZrO_2 has been favored for DRAM capacitor applications because it can obtain a higher *k* phase crystal structure, tetragonal or cubic phase, in the as-deposited state [21]. The *k* values of HfO_2 and ZrO_2 depend on the crystal structure, i.e., monoclinic, and tetragonal or cubic [22, 23]. Because tetragonal or cubic phases are thermodynamically stable at much higher temperatures (about 900 °C) at atmospheric pressure, the films deposited by ALD techniques generally have a monoclinic phase crystal structure [24, 25, 26]. Transition of the monoclinic phase to metastable phases and the accompanying increase in *k* values are quite difficult (results related to this will be discussed in section "Dopant-mediated crystallinity enhancement"). Fortunately, ZrO_2 deposited by the ALD technique exhibits a higher *k* phase (tetragonal) in the as-deposited state, and further crystallization into the tetragonal phase is easily demonstrated by thermal treatment [21].

The carrier conduction mechanisms in ZrO_2 have been investigated to determine an effective way of reducing leakage current (Fig. 3) [27]. As shown in Fig. 3, there is a characteristic difference in the carrier conduction mechanism between ZrO_2 and classical SiO_2 and SiON insulators. First, current conduction by direct tunneling is not observed, and contributions from Schottky emission are not significant. These are attributed to the increased physical thickness and the relatively high E_g of ZrO_2. The E_g values of ZrO_2 are 5.5–6.0 eV, which are smaller than those of classical insulators. However, they are sufficient to create a conduction band offset (CBO) of ~2 eV with a metal electrode (typically TiN or W) [27, 28, 29, 30, 31, 32], resulting in suppression of leakage current by Schottky

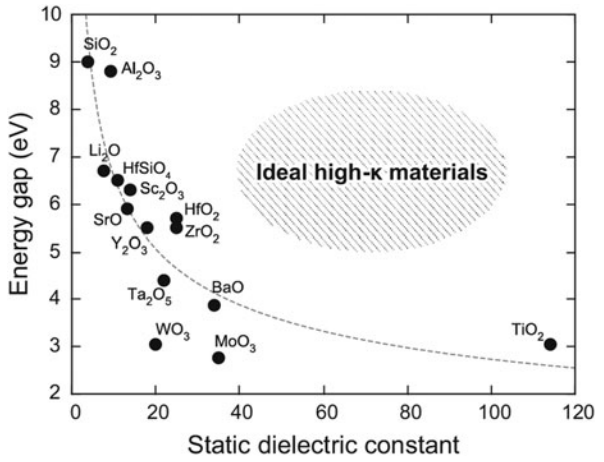

Figure 1: Band gap versus dielectric constant of various high-*k* materials. [Reprinted with permission from Ref. 11 under CC BY-NC-SA 4.0 license. Copyright (2015) Springer Nature.]

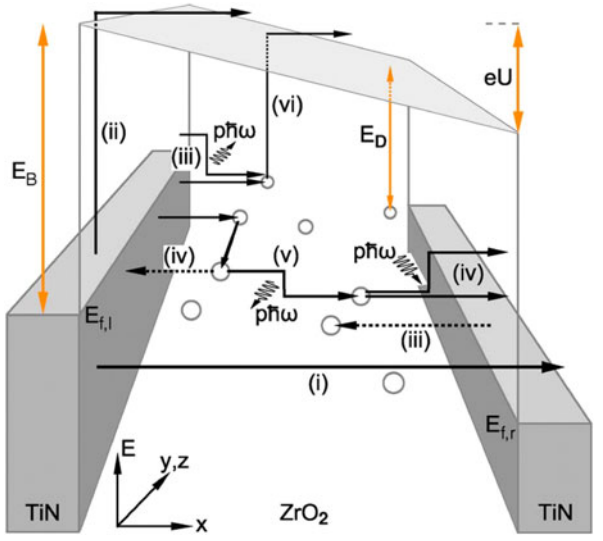

Figure 2: Various leakage current conduction mechanisms on high-*k* material. [Reprinted with permission from Ref. 6. Copyright (2010) IEEE.]

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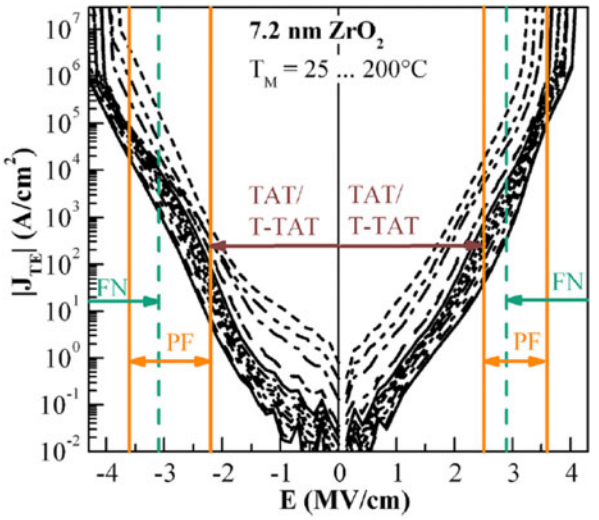

Figure 3: Dominant leakage current conduction mechanism depicted on *J–E* curves of the 7.2 nm thick ZrO_2 thin film. [Reprinted with permission from Ref. 27. Copyright (2013) AIP Publishing.]

emission. Consequently, carrier conduction in ZrO_2 is mediated by TAT (or temperature-activated TAT, T-TAT), P–F, and F–N mechanisms in low, middle, and high electric field (E-field) regions, respectively. These mechanisms are not related to the interface between the insulator and electrode but strongly depend on the bulk properties of the insulator [33] defects such as oxygen vacancies (V_O) [34], grain boundaries [27, 35], and impurities [36]. Grain boundaries were assumed to be the dominant carrier conduction paths. Moreover, ZrO_2 thin films deposited using the ALD technique tend to have a columnar structure in the direction of film growth [37, 38, 39]; this is the same as the electron drift direction in the applied E-field. Martin et al. reported the results of carrier conduction in pristine ZrO_2 thin films observed by conductive atomic force microscopy (C-AFM) measurements [35]. Here, the "trench" on the film surface, which is formed by interconnected grain boundaries, coincides with the location of carrier conduction [Fig. 4(A)], illustrating the role of the grain boundary in carrier conduction. Consequently, various ways of engineering the grain boundary structure in the film have been suggested to suppress the leakage current of ZrO_2. Creating a tortuous carrier conduction path by reducing the grain size would reduce leakage current. But basic approaches such as interrupting the path by inserting an amorphous layer in the middle of the ZrO_2 thin film or eliminating the grain boundary by inducing an amorphous phase in the ZrO_2 itself would be more efficient for reducing leakage current. Accordingly, the $ZrO_2/Al_2O_3/ZrO_2$ (ZAZ) stacked structure, which was designed to reduce the path by integrating amorphous Al_2O_3 in the middle of ZrO_2, was investigated in 2006 [40]. Indeed, this structure demonstrated excellent properties for DRAM devices with a 45 nm design rule. Al_2O_3 was inserted into the middle of the ZrO_2 layer at a certain thickness (more than 0.5 nm) as a distinctive layer [TEM images in the insets of Figs. 4(B) and 4(C)], resulting in suppression of excessive grain growth during crystallization of ZrO_2 as inferred from a dramatically reduced roughness of the ZAZ film [Fig. 4(B)] [41]. Therefore, the leakage current of an MIM capacitor with a ZAZ insulator was significantly reduced compared with that of a ZrO_2 insulator in an applied bias range of −2 to +1.5 V [Fig. 4(D)] [41]. Indeed, a conductive atomic force microscopic (c-AFM) image of the ZAZ film [Fig. 4(A)] showed that the number of carrier conduction paths significantly decreased [35]. Additionally, the range of applied bias with reduced leakage current was consistent with the range in which leakage current conduction of ZrO_2 was governed by trap-related carrier conduction mechanisms (TAT and P–F) (Fig. 3). This implies that Al_2O_3 (with distinctive layer formation) can act as a carrier conduction barrier because of its relatively thick band gap of 9.0 eV [Fig. 5(a)] [31]. Generally, an Al_2O_3 layer has been used as a barrier to carrier conduction by the CBO-related leakage currents (Schottky emission or F–N tunneling). In this regard, the location of the Al_2O_3 inserted to reduce leakage current tends to be at the interface between the metal electrode and the insulator. However, as shown in the ZrO_2 case, inserting Al_2O_3 at the interface is not always the most effective way of using Al_2O_3 for the leakage current reduction. The leakage current asymmetry in $HfO_2/Al_2O_3/HfO_2$ was demonstrated with respect to the location of the inserted Al_2O_3 layer [42]. A 1.2 nm thick Al_2O_3 layer was inserted at various locations in the 5 nm thick HfO_2 film. The current density decreased with the Al_2O_3 layer distance from the electron injection electrode (i.e., cathode), rather than at the interface between the electrode and HfO_2 layer. Also, the work function of the electrode did not affect the asymmetry of MIM diodes. Indeed, the change in CBO with the location of the inserted Al_2O_3 is opposite that of the leakage current behavior [Figs. 5(b) and 5(c)]. This result implies that carrier conduction in the HfO_2 film is governed by a bulk-related conduction mechanism, i.e., P–F emission. Furthermore, the Al_2O_3 layer provides a barrier to bulk conduction. Thus, inserting an Al_2O_3 layer in the middle of the insulator is a more favorable way to interrupt carrier conduction through the conduction band for a bulk conduction-dominant insulator. As shown in the schematic energy band diagram [Figs. 5(d) and 5(e)], conduction of detrapped carriers in the conduction band from the trap site of the insulator, i.e., the carrier produced by the P–F emission mechanism, was blocked by the inserted Al_2O_3 layer. The leakage current reduction caused by insertion of the Al_2O_3 layer is strongly influenced by the carrier conduction mechanism of the insulator. In other words, the method of using the Al_2O_3 layer for reducing leakage current should be changed depending on the carrier conduction mechanism of the insulator.

ZrO_2 and HfO_2 insulators are dominated by bulk-limited leakage conduction; therefore, using a metal electrode with

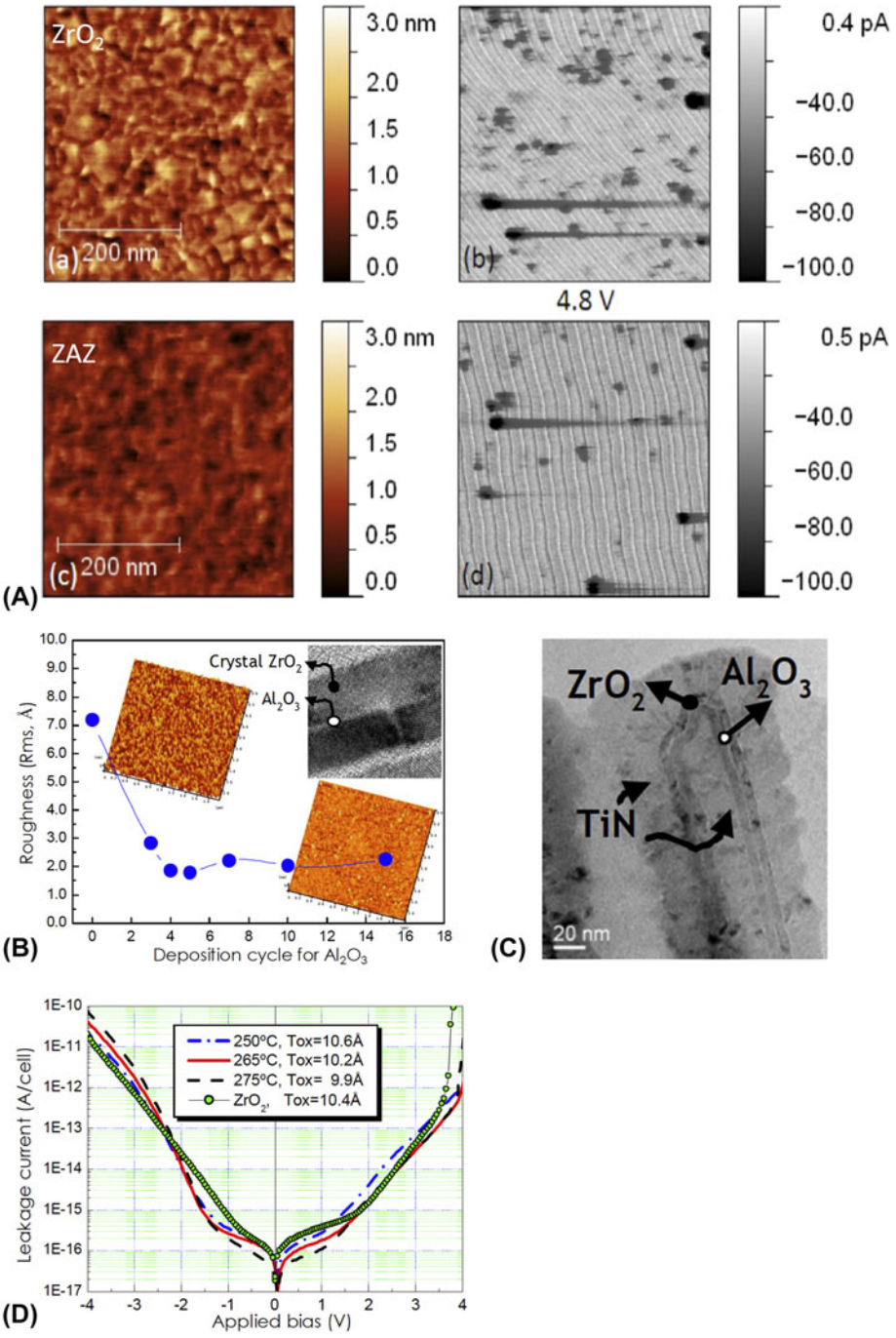

Figure 4: (A) AFM and c-AFM image of ZrO_2 and ZAZ thin films. [Reprinted with permission from Ref. 35. Copyright (2013) AIP Publishing.] (B) Roughness of the ZAZ thin film with respect to the deposition cycle of Al_2O_3 (inset) cross section TEM image of the ZAZ thin film. (C) Cross section TEM image of the TiN/ZAZ/TiN DRAM capacitor structure. (D) *I–V* curves of MIM capacitors using ZrO_2 and ZAZ as an insulator layer. [Reprinted with permission from Ref. 41. Copyright (2006) IEEE.]

a higher work-function does not result in any significant improvement in leakage current. An et al. reported that the leakage current of an MIM capacitor with a ZAZ film was successfully reduced by using a Ru electrode (a noble metal electrode) rather than a TiN electrode [43]. However, it should be noted that the leakage current reduction did not originate from the relatively higher work-function of the Ru electrode than that of TiN. When the top electrode was changed from TiN to Ru, the leakage current density due to electron injection from the bottom electrode decreased significantly compared with that of the TiN top electrode sample only in the specific electric field region of 1–2 MV/cm, even though the bottom

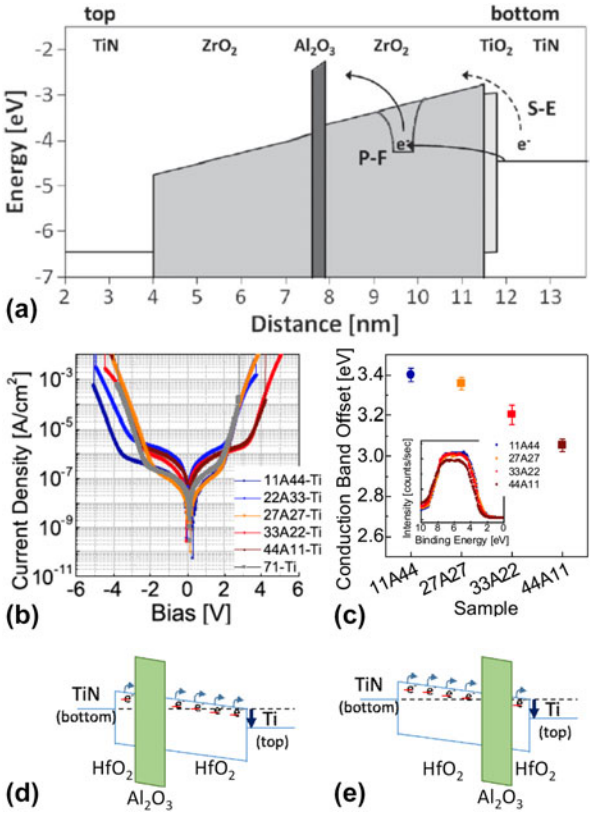

Figure 5: (a) Simulated energy-band diagram of a 7.5 nm TiN/ZrO_2/Al_2O_3/ZrO_2/TiO_2/TiN stack, showing schematically Poole–Frenkel emission and Schottky-emission. [Reprinted with permission from Ref. 31. Copyright (2014) IEEE.] (b) *J*–*V* curves and (c) the CBO of (bottom) TiN/HfO_2–Al_2O_3–HfO_2/Ti (top) with various Al_2O_3 inserting location (inset) valence band spectra of the HfO_2–Al_2O_3–HfO_2 films on TiN (left-bottom). [Reprinted with permission from Ref. 42. Copyright (2019) IEEE.] (d) and (e) Schematic energy band diagram of TiN/HfO_2–Al_2O_3–HfO_2/Ti capacitors.

electrode was the same (TiN for both Ru and TiN top electrodes) [Fig. 6(a)]. This unprecedented behavior was due to the change in oxygen vacancy density in the ZAZ film, which induces P–F emission through the reaction with active oxygen during Ru top electrode fabrication. The same behavior was observed in comparison with TiN, RuO_2, and Pt metal used as a top electrode for TiN/ZAZ MIM capacitors [34]. As shown in Fig. 6(b), the leakage current density caused by electrons injected from the bottom electrode was changed with respect to the used top electrode materials, even for the same TiN bottom electrode. Moreover, the MIM capacitor with a Pt top electrode exhibited a higher leakage current density in a specific electric field region (where the P–F emission governs the leakage current density) than that of the RuO_2 top electrode sample, even though the work-function value of RuO_2 is lower than that of Pt. This result also indicates that adapting a treatment for reducing defects in the bulk is an effective way to reduce the leakage current of ZrO_2 or HfO_2 due to grain boundaries or oxygen vacancies, rather than for changing the barrier height at the interface.

Usually, the contribution of the interface increases with decreasing film thickness as the ratio of the interface increases. However, the contribution of the bulk-related terms to the leakage current paradoxically increased for MIM capacitors with ZrO_2 or HfO_2 as the physical thickness of the insulator decreased. The asymmetry in leakage current with respect to the location of the inserted Al_2O_3 layer [Fig. 6(c)] was not observed when the total film thickness was increased to 9 nm [27]. As shown in Fig. 6(d), a reduction in leakage current was only exhibited for a ZAZ film thickness of 4.6 nm [43]. These results imply that engineering grains or defects are becoming more important. Additionally, as the design rule decreases, the total thickness of the ZAZ film decreases, meaning that it is impossible to insert an Al_2O_3 layer as a distinctive layer. The number of ALD cycles of Al_2O_3 in a ZAZ film is less than 4–5 cycles. Thus, it should be considered as a dopant rather than a distinctive layer. Thus, the Al_2O_3 in ZAZ cannot block the carrier conduction path in ZrO_2. However, the ZAZ film with dopant level Al_2O_3 concentration provides an adequate leakage current level for DRAM capacitor applications. This indicates that even a small amount of Al_2O_3 can successfully suppress carrier conduction in ZrO_2. The reason for this is related to crystallization. Crystallization occurs through stages of nucleus formation and coalescence. In the thin film process, the nucleus generally formed on the substrate surface in the very early stages, followed by coalescence during film deposition, resulting in deposited films with a columnar structure [44, 45]. This columnar structure forms a grain boundary along the thickness direction of the thin film, which coincides with the direction of the applied electric field, making it vulnerable to leakage current. The effective leakage current suppression by the inserted Al_2O_3 layer in the ZrO_2 layer is actually related to intersections in the grain boundary along the thickness direction. However, when Al_2O_3 was used as a dopant, it inhibited coalescence of the dielectric, resulting in a smaller grain crystal structure of the matrix dielectric. In this regard, a "mesocrystalline" structure was suggested for reducing leakage current [25, 46]. The mesocrystalline structure consisted of partially crystallized grains incorporated in an amorphous matrix. This structure helps enhance the dielectric constant and reduce leakage current by partially crystallized grains in the remaining amorphous matrix, which eliminate the grain boundaries and their network, respectively [25]. This structure shows that the dopant (Al_2O_3 in this case) cannot hinder nucleation but can suppress coalescence. The ZrO_2 thin film can form nuclei during the deposition process. This is followed by coalescence of nuclei during the continued deposition process, resulting in enhanced crystallinity with increasing thin film thickness. However, when dopants such as Al_2O_3 are added in the ZrO_2 thin film, the grain size is reduced compared with that of the pristine ZrO_2. Dopants in

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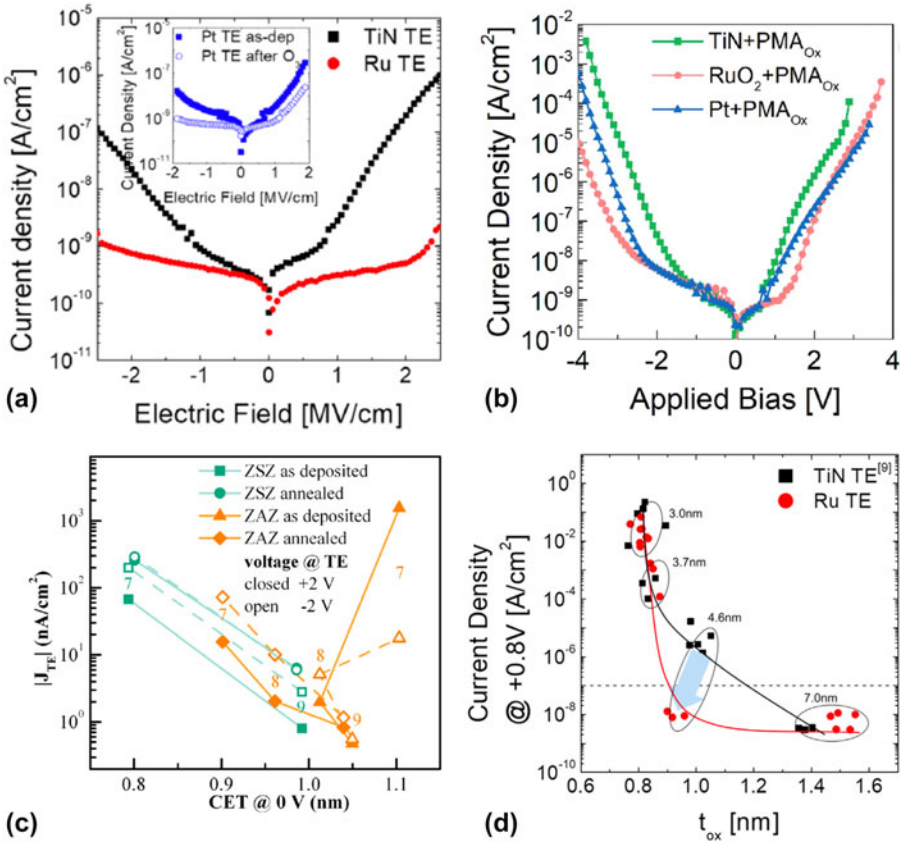

Figure 6: (a) *J–E* characteristics of the MIM capacitors with different top electrodes (inset): *J–E* characteristics of the MIM capacitors with the (opened) Pt top electrode and (closed) Pt top electrode and using O_3 treatment. [Reprinted with permission from Ref. 43. Copyright (2019) John Wiley and Sons] (b) *J–V* curves of MIM structures consisted of TiN for the bottom electrode, 5 nm thick ZAZ for the insulator, and TiN (blue), RuO_2 (green), and Pt (red) for the top electrode, respectively. [Reprinted with permission from Ref. 34. Copyright (2018) IEEE.] (c) Leakage current density measured at the top electrode (J_{TE}) in dependence of the CET at 0 V of MIM capacitors with TiN electrodes and as deposited and annealed (PDA at 650 °C for 20 s in N_2) ZSZ, and ZAZ films as the dielectric. The included numbers reveal the nominal layer thicknesses. [Reprinted with permission from Ref. 27. Copyright (2013) AIP Publishing.] (d) Variations in *J* as a function of t_{ox} at a +0.8 V applied voltage. The solid lines were added for eye guidance. [Reprinted with permission from Ref. 43. Copyright (2019) John Wiley and Sons.]

ZrO_2 or HfO_2 also operate by forming a winding conduction path (by reducing the grain size or eliminating the grain boundary) by inducing an amorphous phase. In this role, the relatively higher band gap of Al_2O_3 (9 eV) does not contribute to reduce the leakage current. This result is contrary to the overall intention of using the Al_2O_3 thin film for reducing leakage current. Indeed, the total thickness of the dielectric is thick enough to use a distinctive layer of Al_2O_3, the band gap of which played a significant role in reducing the leakage current. However, as the design rule has decreased, the physical shape of Al_2O_3 in the dielectric changed from a layer to a dopant, and the resulting role of Al_2O_3 in reducing leakage current has changed, even though the community may not be aware of it. Consequently, there is no reason to continue to use Al_2O_3 in the era of dielectric physical thickness less than 5 nm. Based on this new finding about the role of Al_2O_3, we can now find alternatives for achieving better performance with ZrO_2. This is the motivation for determining the exact mechanisms of carrier conduction in dielectrics before developing new dielectric materials or processes.

Interface-related leakage current conduction

A critical trade-off relationship in high-*k* dielectrics is that increasing the dielectric constant results in a decreased band gap, and all research works have suffered from this (Fig. 1). As a consequence, the CBO, i.e., the barrier height between the metal electrode and dielectric, decreased with the increasing dielectric constant, resulting in a decrease in dielectric strength. In other words, the contribution of interface-related leakage current conduction to overall leakage conduction in the dielectric increases when using higher-*k* dielectric thin films. This implies that the approach using a higher *k* dielectric for reducing leakage (such as ZrO_2 and HfO_2) does not result in any significant leakage current reduction for high-*k* dielectrics.

ZAZ-like approach for TiO_2

TiO_2 is one of the most extensively studied high-k materials for dielectric materials in DRAM capacitors because of its higher dielectric constant of ~40 or ~100 for anatase and rutile crystal structures, respectively [47]. On the other hand, the band gap of TiO_2 is quite narrow (3.3 and 3.0 eV for anatase and rutile phase, respectively) [48, 49]. Thus, TiO_2 has shown poor results for several decades because of its severe leakage current problem. Meanwhile, the ZAZ structure was the most successful example among the various suggested attempts for reducing leakage current of high-k dielectrics. The ZAZ-like approach for reducing leakage current is summarized by these two strategies: (i) cutting the leakage path by inserting an Al_2O_3 layer with fully crystallized ZrO_2 or (ii) minimizing grain size or forming amorphous ZrO_2 by using Al_2O_3 as a dopant. In this regard, the ZAZ-like approach has been demonstrated on TiO_2. Jeon et al. prepared various structures of TiO_2 and Al_2O_3 by changing the crystal structure of TiO_2 and position of Al_2O_3 (i.e., layer of the dopant) [50].

First, the electrical properties of a TiO_2–Al_2O_3 mixed (Al-doped TiO_2) and laminated (TiO_2–Al_2O_3–TiO_2) film structure were investigated for suppressing crystallization of TiO_2 by inserting an Al_2O_3 layer. In case of the mixed structure, an Al_2O_3 layer thickness greater than 10 nm can effectively suppress crystallization of TiO_2, resulting in a dramatic reduction in leakage current density from $\sim10^{-3}$ to $\sim10^{-7}$ A/cm^2 [Fig. 7(a)]. However, the dielectric constant also significantly decreased below 30, which is comparable with that of ZrO_2 and HfO_2, because of severe crystallinity degradation. This makes it difficult to find any reason for using TiO_2 instead of ZrO_2 or HfO_2. Most of all, the difference in k values between the crystalline phase and amorphous phase increased for dielectrics with a high-k value. The laminated film structure also exhibited only a dielectric constant under 50 [Fig. 7(b)]. Therefore, the ZAZ-like approach resulted in more disadvantages than advantages in the case of TiO_2. Moreover, the electrical properties of the TiO_2–Al_2O_3 mixed film structure (i.e., using Al_2O_3 as a dopant) should be emphasized. In the case of ZrO_2, merely doping with Al_2O_3 can suppress the leakage current effectively. By contrast, when Al_2O_3 was doped in TiO_2 with a same level of Al concentration in ZrO_2 cases, no enhancement in leakage current was observed. The Al_2O_3 dopant in TiO_2 would also suppress coalescence of grains of TiO_2, which might suppress carrier conduction through the grain boundary, i.e., bulk-related leakage current. However, the lack of enhancement in leakage current by the Al_2O_3 dopant implies that the dominant carrier conduction mechanism of TiO_2 is not related to the bulk.

Al-doped TiO_2

Kim et al. reported an exceptional result related to leakage current reduction in TiO_2 thin films [51]. The leakage current of a rutile phase TiO_2 thin film obtained using a Ru bottom electrode and an O_3 source for the TiO_2 ALD process decreased by about 10^5–10^6 times with a few at.% of Al doping [Fig. 8(a)]. Finally, a minimum equivalent oxide thickness of 0.5 nm was achieved in this Al-doped TiO_2 (ATO) thin film because of the significant contribution of appropriate Al doping, which reduced leakage current by ~10^5 times. The dielectric constant for this ATO thin film was ~60, which was significantly smaller than the expected ~100 for a rutile phase because of the decrease in crystallinity from the Al dopant. The tremendous leakage current reduction in this report was likely because Al doping increased the CBO to its ideal value via the acceptor-like characteristics of the Al ions in the TiO_2 [52, 53].

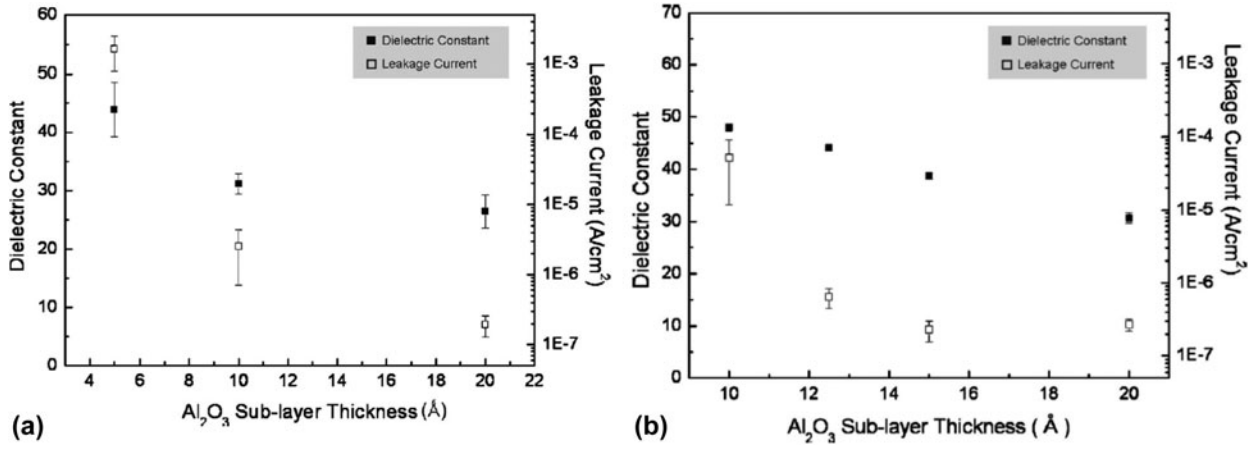

Figure 7: (a) Dielectric constant and leakage current of TiO_2/Al_2O_3 mixed films. The TiO_2 sublayer thickness is 40 Å, and the Al_2O_3 sublayer thickness is 5, 10, and 20 Å, respectively. (b) Dielectric constant and leakage current of anatase-TiO_2/Al_2O_3/anatase-TiO_2 films. The TiO_2 sublayer thickness is 40 Å, and the Al_2O_3 sublayer thickness is 10, 12.5, 15, and 20 Å, respectively. [Reprinted with permission from Ref. 50. Copyright (2008) The Electrochemical Society.]

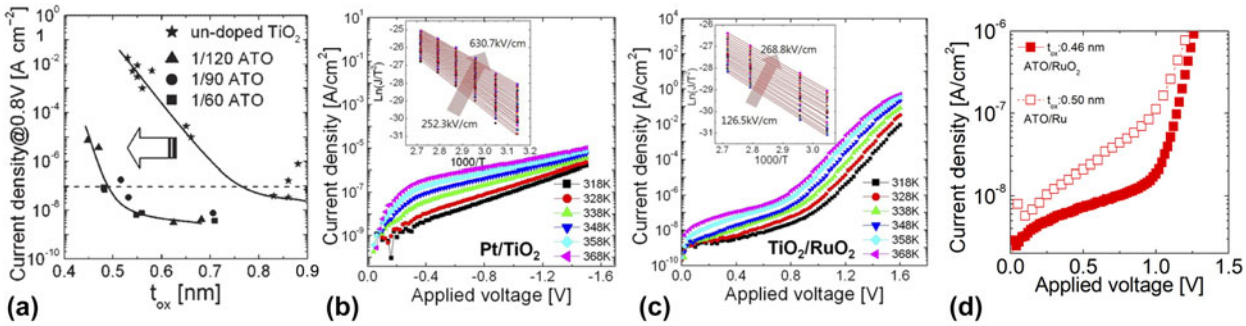

Figure 8: (a) J @ 0.8 V versus t_{ox} for the TiO_2 and Al-doped TiO_2 thin films with various subcycle ratio. [Reprinted with permission from Ref. 51. Copyright (2008) John Wiley and Sons.] (b) The negative and (c) positive J–V characteristics of the $Pt/TiO_2/RuO_2$ capacitor with elevating measurement temperature from 318 to 368 K (inset in b and c). (d) Change in the leakage current density of the $Pt/ATO/RuO_2$ (or Ru) capacitors as a function of the applied bias voltage. [Reprinted with permission from Ref. 54. Copyright (2011) AIP Publishing.]

Moreover, the leakage current reduction observed when using a higher work-function electrode also indicates that the overall leakage current density of ATO dominantly depends on the CBO [Figs. 8(b)–8(d)] [54]. According to this suggested mechanism that only focuses on the interface, there is no reason to homogeneously dope the Al throughout the whole thin film. Consequently, evaluation of the leakage current reduction mechanism in the rutile TiO_2 was performed by changing the location of the Al doping in the dielectric film.

These results [53, 55] showed that the electrical properties of ATO depended on the Al doping profile. Specifically, an asymmetric Al doping profile along the film thickness direction induced characteristic behavior in leakage current density versus electric field (J–E) and capacitance versus voltage (C–V) plots (Fig. 9). These characteristic behaviors are solely related to the changes in CBO values with respect to the concentration of the Al dopant at the interface of the ATO and electrode. The leakage current density in the $-1.0 \sim +1.0$ MV/cm range was determined by Al concentration at the interface where the electrons were injected [i.e., at the bottom interface when a positive bias was applied on the top electrode, Fig. 9(A)]. Moreover, a hump with a significant slope change was observed in the J–E plot for samples with the lowest Al concentration at the electron–injection interface. This hump provides evidence that only the Al dopant at the interface increases the barrier height, resulting in a decrease in leakage current. A different Al concentration induces a barrier height difference between the two interfaces. An internal bias originating from the barrier height difference is induced, and the presence of such a barrier height difference distorts the J–E plots. Moreover, this result revealed that the CBO increases because of Al doping only in the TiO_2 thin film having a rutile crystal structure, not in the anatase-phase TiO_2 thin film [Fig. 9(B)] [53]. This difference originated from the difference in energy levels of the Al^+ dopant with respect to the crystal structure of the TiO_2 thin film, indicating that the CBO governs the entire leakage current density level in TiO_2 thin films. The internal bias caused by the Al concentration difference between two interfaces also induced a distortion in the C–V plot [Fig. 9(C)] [55]. It is common to observe a decrease in the C value in small signal C–V measurements under a high DC bias in an MIM capacitor with a high-k dielectric as an insulator. Therefore, the maximum C value is generally observed at an applied bias of 0 V. However, the asymmetry of the Al concentration induced a shift in V_{max}, the applied bias value where the maximum C is observed, from 0 V to a point corresponding to the internal bias voltage that could be induced by different Schottky barrier heights between two interfaces. The ~ -0.1 V ($+0.1$ V) shift in V_{max} of the 0 A (250 A) sample revealed that the barrier height at the bottom interface was higher (lower) than that of the top interface. From the aforementioned results, it was concluded that the leakage current density of the MIM capacitor with ATO thin films is governed by the barrier height at the interface of the insulator and metal electrode, which can be altered by the Al dopant concentration at the interface but not in the bulk region. This is the opposite result from that observed in the ZrO_2 case, wherein the Al dopant in the bulk region is responsible for leakage current reduction. This difference in the effect of the Al dopant on leakage current for ZrO_2 and TiO_2 originated from the difference in the dominant carrier conduction mechanism in ZrO_2 (bulk-related) and TiO_2 (interface-related).

$SrTiO_3$

$SrTiO_3$ (STO) has also attracted a lot of attention as one of the most promising dielectric materials, offering an extraordinarily high dielectric constant of ~300 because of its perovskite crystal structure [56, 57, 58]. However, the MIM

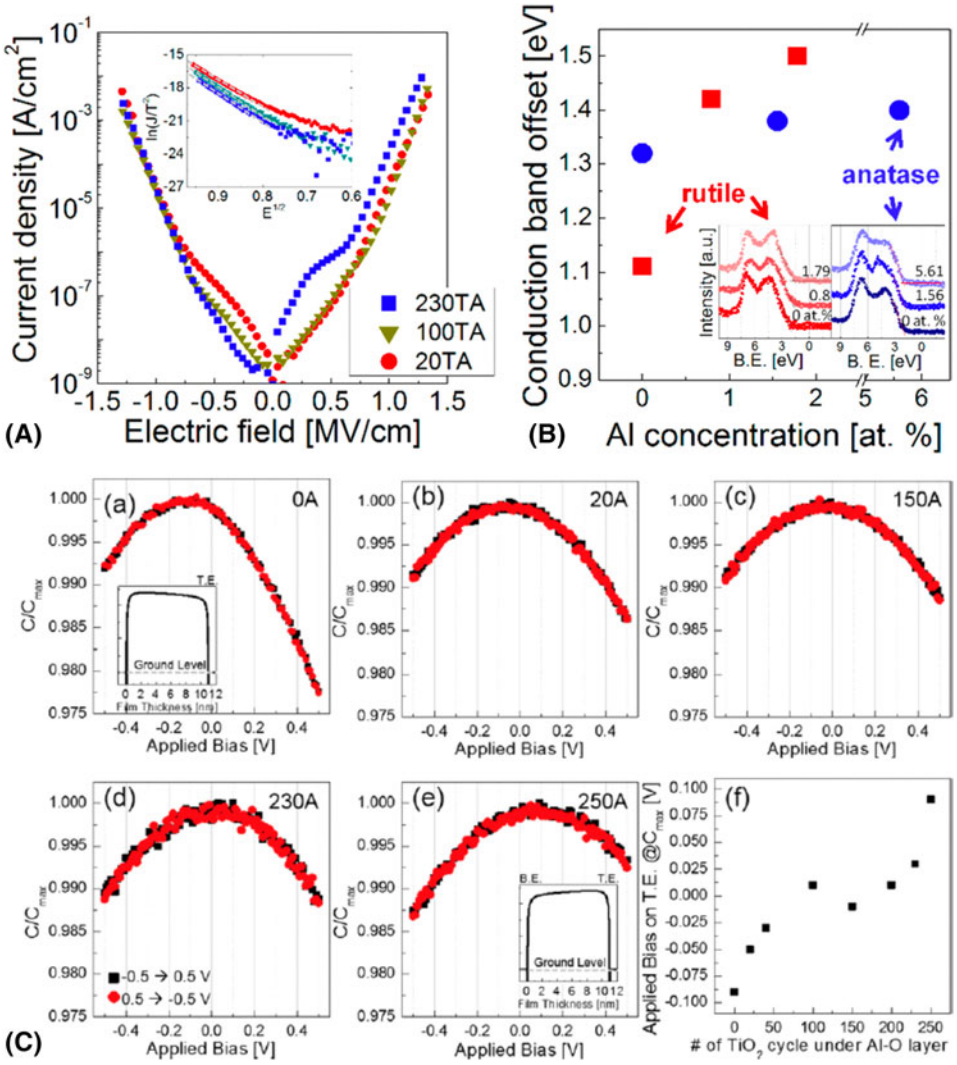

Figure 9: (A) *J–V* curves of the ATO samples with various Al locations (inset) $\ln(J/T^2)$ versus $E^{1/2}$ plots of the low–electric field region to confirm the Schottky emission mechanism. (B) Variation of the CBO as a function of the Al concentration of rutile (red) and anatase (blue) TiO_2. The left and right panels of the inset show the valence band spectra of the rutile and anatase TiO_2 films, respectively. [Reprinted with permission from Ref. 53. Copyright (2014) American Chemical Society.] (C) *C–V* curves of the various ATO films. The number in each graph indicates the number of TiO_2 ALD cycles before the single Al_2O_3 ALD cycle was commenced (right-bottom). Applied bias on the top electrode where the maximum capacitance was acquired for various ATO films. [Reprinted with permission from Ref. 55. Copyright (2015) John Wiley and Sons.]

capacitor with STO also suffers from severe leakage current problems based on the trade-off relationship between the dielectric constant and band gap. The dominant reason for severe leakage current problems in STO thin films is related to its narrow band gap of 3.2 eV. Therefore, carrier conduction in STO thin films deposited by pulsed laser deposition techniques (which can offer a relatively perfect crystal structures) occurs through the Schottky emission mechanism, as in TiO_2, which also has a very narrow band gap [Fig. 10(a)] [59]. However, defect-related mechanisms (i.e., bulk-related, such as TAT or P–F emission) become the dominant mechanisms of carrier conduction in STO thin films deposited by ALD [Figs. 10(b) and 10(c)] [60, 61]. This is because ALD techniques result in imperfect ternary oxide deposition. Even when the band gap of STO is as narrow as that of TiO_2, the carrier conduction mechanism would not be the same as that of TiO_2. In other words, it is difficult to anticipate the carrier conduction mechanism based only on the band gap of the dielectric film.

Summary

Based on the previous results, there is no absolute solution for controlling leakage current for all high-*k* dielectric materials. Although use of Al_2O_3 has been considered a universal solution for reducing leakage current reduction, dramatic leakage current reduction by Al_2O_3 was achieved only for some cases of high-*k* dielectrics, such as ZrO_2 and rutile-TiO_2. Although

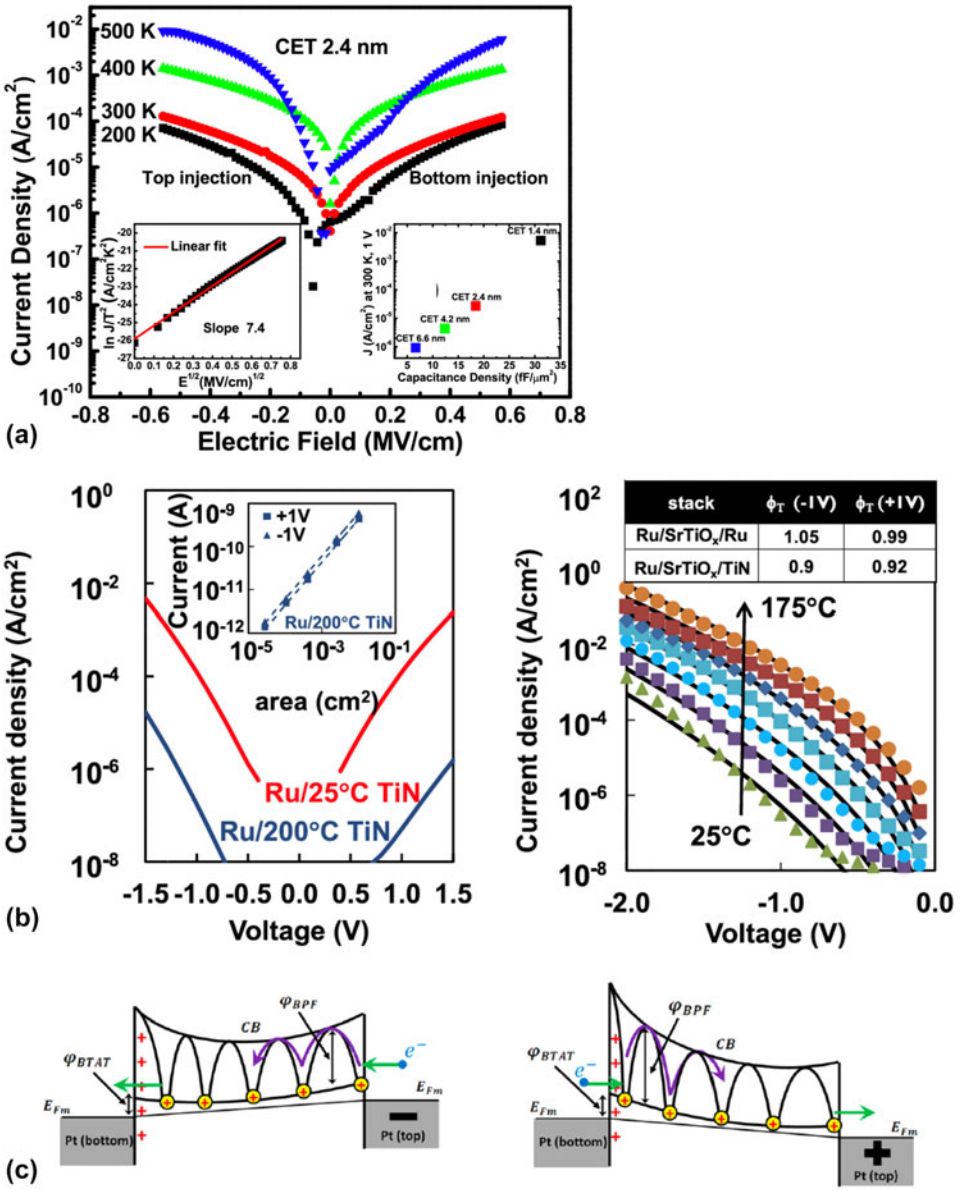

Figure 10: (a) Leakage current density of the dielectric stack with a CET value of 2.4 nm measured at four different temperatures. (inset-left) Room-temperature Schottky plot for the stack with a CET value of 2.4 nm. (inset-right) Leakage current values of the four stacks versus capacitance density measured at 300 K and at 1 V. [Reprinted with permission from Ref. 59. Copyright (2016) AIP Publishing.] (b) (left) Current density as a function of the gate bias for the Ru/$SrTiO_x$/Ru stack with TiN deposited at 25 and 200 °C. (inset) Current as function of capacitor area, (right) current density as a function of the gate bias measured at different temperatures (symbols) and fitted using the Poole–Frenkel model (lines). (inset) The extracted Poole–Frenkel trap depth at + and −1 V. [Reprinted with permission from Ref. 60. Copyright (2014) IEEE.] (c) (left) Negative voltage bias at the top electrode and low injection of electrons to the bottom electrode due to the large distance of oxygen vacancies from the bottom electrode. (right) Positive voltage bias at the top electrode and high injection of electrons to vacancies due to the small distance between oxygen vacancies and the bottom electrode. [Reprinted with permission from Ref. 61. Copyright (2012) AIP Publishing.]

the obtained leakage current reduction results were the same for these two dielectrics (i.e., ZrO_2 and rutile-TiO_2), the mechanisms were quite different. Moreover, there are no absolute criteria governing the carrier conduction mechanisms in high-*k* dielectrics. At a glance, band gap appears to be a definitive criterion for determining the dominant carrier conduction mechanism. That is, carrier conduction is bulk-related for a relatively higher band gap and interface-related for relatively lower band gap high-*k* dielectrics. However, as in the STO case, the bulk-related carrier conduction mechanism can cause a dominant overall leakage current for narrow band gap high-*k* dielectrics when the dielectric has many bulk defects caused by the deposition technique. Therefore, an exact carrier conduction mechanism evaluation should be conducted in advance for the targeted dielectric to develop an effective method to reduce leakage current.

Capacitance density

Higher capacitance density is desirable for robust operation of all electronic devices that use capacitor components. Capacitance density is related to the polarization of a dielectric material as represented by the dielectric constant. However, in an actual MIM capacitor, the measured capacitance density is generally lower than expected. The difference between actual and ideal capacitance is likely caused by the polycrystalline nature of the deposited thin film and the crystallinity degradation in the surface region. In this regard, research on enhancing the capacitance density has focused on increasing the crystallinity of the thin film and eliminating the influence of the interface region.

Increasing the crystallinity

The polycrystalline nature of deposited thin films decreases the actual dielectric constant. However, achieving a single crystal insulator by a deposition technique is theoretically impossible and is not favorable from a processing perspective. Therefore, approaches for inducing a high-*k* crystal structure and increasing the proportion of the crystallized region have been investigated as effective solutions for enhancing the capacitance density in MIM capacitors.

Dopant-mediated crystallinity enhancement

Most high-*k* dielectrics have various crystal structures, and the dielectric constant also varies with respect to the crystal structure. Deposited HfO_2 and ZrO_2 films typically exhibit three crystal structures of monoclinic, tetragonal, and cubic phases with dielectric constants of 20, 30–50, and 30, respectively [24, 26], indicating that capacitance density could be changed considerably with respect to the crystal structure of the deposited film. The tetragonal phase has the highest dielectric constant crystal structure and is readily obtained in the ZrO_2 deposition process [Fig. 11(a)]. However, the deposited HfO_2 thin film generally has the lowest dielectric constant crystal structure of the monoclinic phase [Fig. 11(b)] [21, 25, 42]. In this regard, various methods for inducing high-*k* phases of HfO_2 have been investigated. Tetragonal and cubic phases are metastable at atmospheric pressure and room temperature. The transition of the monoclinic phase to these metastable phases requires application of an internal stress that acts as a driving force for the transition from the monoclinic, low-symmetric phase to the tetragonal and cubic high-symmetric phases [23]. Based on this understanding, several methods, such as cation doping [21, 25, 62, 63, 64], carbon impurity incorporation [65], production of oxygen-deficient phases [66], and alloying of ZrO_2 and HfO_2 [67, 68], have been suggested. Among them, cation doping is the most favorable method because it can simultaneously reduce leakage current. In this regard, various cations have been used as dopants of HfO_2 to obtain high-*k* phases. Doping of Al_2O_3 has attracted a lot of attention because of its relatively wide band gap, which produces an expectation of leakage current reduction. Results of the enhanced dielectric constant (up to ~40) and improved leakage current achieved by Al doping into HfO_2 thin films have been reported in various device applications, such as DRAM capacitor dielectrics and gate insulators [Fig. 11(c)] [21, 25, 64]. It should be noted that the dielectric constant gradually increases with increasing Al concentration to a specific concentration value and decreases to the level of pristine HfO_2 as Al exceeds this specific concentration [Figs. 11(c)–11(e)]. This is because of the phase transition in HfO_2 thin films from monoclinic to tetragonal or cubic and finally to amorphous with increasing Al concentration. The mechanism of the phase transition was revealed by first-principle calculations based on the density functional theory that the relative phase stability changed with the Al concentration [Fig. 11(f)] [25, 62]. From the calculation, the most stable phase is changed from monoclinic to tetragonal and cubic with increasing the Al concentration in HfO_2. The critical grain size (CGS) can also be used to explain this phase transition behavior, especially in the difference between ZrO_2 and HfO_2 [65, 69, 70, 71, 72, 73]. The CGS is the grain size of the dielectric film where the transition occurs from tetragonal or cubic to monoclinic based on surface energy and phase stability. The CGS for the ZrO_2 film was ~25–30 nm, resulting in thin films with tetragonal and cubic phases in the as-deposited state. However, the only ~5–10 nm CGS of HfO_2 indicates the need for a dopant to obtain a high-*k* phase. Furthermore, phase engineering using a dopant has recently attracted a lot of attention for demonstrating ferroelectric HfO_2 thin films.

Crystallinity coherency with the electrode

Another effective way to enhance the crystallinity of dielectric films is to induce epitaxial growth due to coherence between crystal structures of the dielectric and electrode substrate during dielectric film deposition. Generally, a crystallized dielectric film has a higher dielectric constant than that of amorphous or low crystalline forms. Hence, crystallization during the deposition process would be favorable to improve capacitance density of the MIM capacitor. However, the temperature of the ALD process is relatively lower than the moderate annealing process temperature. Therefore, ways to increase the process temperature to induce crystallization during the deposition process have been suggested, although this might result in degradation to the thermal budget of the device. Moreover, most high-*k* dielectrics have two or more

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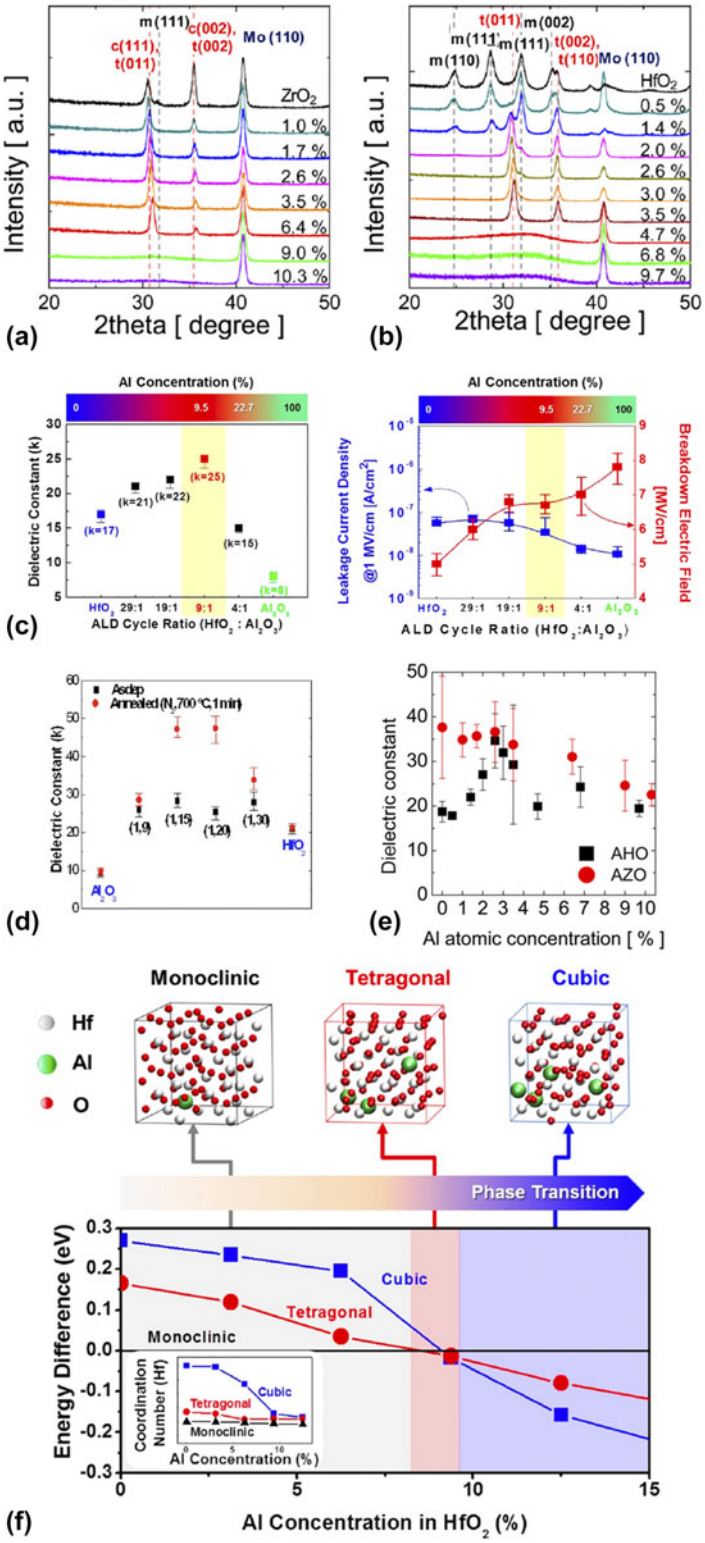

Figure 11: GAXRD patterns of the postannealed (a) Al-doped ZrO_2 and (b) Al-doped ZrO_2 films with different Al concentrations. [Reprinted with permission from Ref. 21. Copyright (2014) American Chemical Society.] (c) Variations in (left) the dielectric constant and (right) leakage current density at 1 MV/cm (blue) and breakdown electric field (red), as functions of ALD cycle ratio between HfO_2 and Al_2O_3 [Reprinted with permission from Ref. 25. Copyright (2016) American Chemical Society.] (d) Dielectric constants of Hf aluminate films with respect to the number of unit cycles in a HfO_2 subcycle before and after the annealing process. [Reprinted with permission from Ref. 64. Copyright (2006) AIP Publishing.] (e) Variations in the dielectric constant of the Al-doped HfO_2 and Al-doped ZrO_2 films as a function of the Al concentration. [Reprinted with permission from Ref. 21. Copyright (2014) American Chemical Society.] (f) Relative stabilities between phases for different Al doping concentrations. [Reprinted with permission from Ref. 25. Copyright (2016) American Chemical Society.]

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representative crystal structures. Unfortunately, higher dielectric constants can be achieved with higher temperature-stable crystal structures. This also makes it difficult to achieve sufficiently high dielectric constants when the thermal budget is applied during the deposition process.

In this regard, epitaxial growth behavior based on coherence between the crystallinity of the substrate and deposited film has been evaluated as the most effective way to obtain highly crystalline high-*k* dielectric thin films with desirable crystalline structures. ALD of TiO_2 thin films on Ru or RuO_2 is a most good example of crystallization of dielectrics facilitated by coherency with the substrate [74]. TiO_2 thin films have three kinds of crystal structures: anatase, rutile, and brookite. Among them, the rutile structure is the most favorable for DRAM capacitor dielectric applications because of its higher dielectric constant of 80–100. However, the rutile structure is difficult to obtain through moderate deposition or annealing processes because of the high temperature stability of rutile crystal structures. Many attempts have been made, but researchers have struggled to achieve the rutile phase. In 2004, Kim et al. reported TiO_2 thin films of the rutile phase at the as-deposited state by the ALD process at a process temperature of 250 °C, which is actually too low to induce rutile phase crystallization. The key factor in this achievement was the use of a Ru film as a substrate and O_3 as an oxygen source in the TiO_2 ALD process. In this case, O_3 introduced in the first stage of TiO_2 ALD oxidized the surface of the Ru substrate to form RuO_2 [Fig. 12(a)]. RuO_2 easily crystallized to the rutile phase with almost identical lattice parameters to that of the rutile phase of TiO_2 thin films. Thus, the deposited TiO_2 thin film on a Ru substrate with O_3 as an oxygen source resulted in a rutile crystal structure in the as-deposited state. When H_2O was used as an oxygen source of TiO_2 ALD instead of O_3, only anatase or amorphous phases were obtained because the weak oxidation potential of H_2O cannot produce RuO_2 on the surface of the Ru substrate during the TiO_2 ALD process [Figs. 12(b) and 12(c)]. This result indicates that coherence of the crystal structure between the substrate film and deposited film, RuO_2 and TiO_2 in this case, is the key factor that allows deposition of a desired specific crystal structure (e.g., rutile-phased TiO_2). The deposition of TiO_2 on RuO_2 is not the only case for crystallinity coherency of dielectric with the electrode. As the same manner, IrO_2, MoO_2, and SnO_2 also can induce the rutile-phased TiO_2 thin film during the ALD process [50, 75, 76, 77]. Consequently, using a substrate that has crystal structure coherency is one of the most effective ways of acquiring high dielectric constants in deposited dielectric thin films.

Defective phase–assisted crystallinity enhancement

Generally, dielectric thin films have amorphous or partially crystallized structures right after the deposition process. Hence,

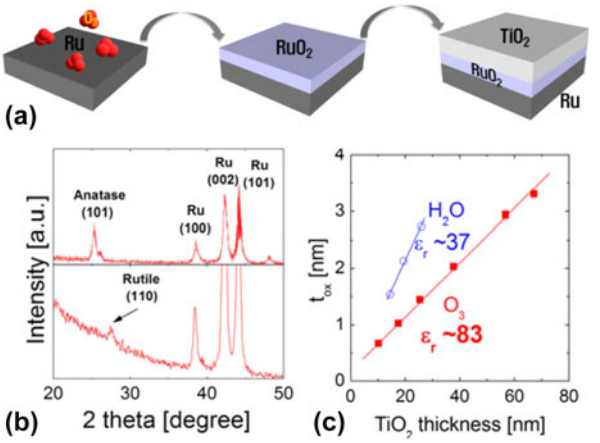

Figure 12: (a) Schematic diagram of the formation of RuO_2 and resulting rutile-phased TiO_2 thin film during TiO_2 ALD with O_3 as an oxidant. (b) XRD spectra of TiO_2 thin film deposited on Ru with (upper) H_2O and (lower) O_3 as an oxidant, respectively. (c) Variations in the oxide equivalent thickness of TiO_2 films grown on Ru with H_2O and O_3 as an oxidant, respectively, indicating bulk dielectric constants. [Reprinted with permission from Ref. 74. Copyright (2004) AIP Publishing.]

particular crystallization processes, such as postdeposition annealing (PDA) or postmetallization annealing (PMA), have been used to enhance or induce a specific crystal structure in deposited thin films. Furthermore, these postannealing processes are also adopted for the formation of stoichiometric compositions of deposited thin films, especially for ternary oxide deposition using the ALD technique [78, 79, 80, 81, 82, 83, 84, 85, 86]. In the ALD process for binary as well as ternary oxides, each atom will have its metastable location in the aspect of potential energy in the as-deposited state. Therefore, the crystal structure of the deposited thin film in the as-deposited state is generally amorphous. The PDA or PMA process is applied to supply additional energy for achieving the designated crystal structure or stoichiometry. Here, the key point is that the purpose of the PDA or PMA process is to apply additional energy to facilitate movement (or migration) of atoms to their own lowest energy positions at a given condition (such as temperature or atmosphere). In other words, there is a kind of energy barrier that should be overcome to transition from the metastable state of the deposited thin film in the as-deposited state to the stable state. Thus, inducing a more unstable as-deposited state would be helpful to obtain the desired final state.

Crystallinity enhancement of $SrTiO_3$ (STO) thin film mediated by defective ALD subcycles has been reported [87]. The STO thin film is a representative ternary oxide deposited by ALD consisted of SrO and TiO_2 subcycles. Stoichiometry is controlled by the subcycle ratio, and the characteristic perovskite crystal structure is achieved by a subsequent PDA process. Developing more robust and stable ALD subcycles is a crucial way of achieving highly crystallized STO thin films by ALD. By

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contrast, Chung et al. reported crystallinity enhancement in STO ALD from a faulty TiO_2 ALD subcycle. During the STO ALD, the deposition behavior of the TiO_2 ALD subcycle is strongly dependent on the nature of the surface terminations, which influence chemisorption of the Ti precursor. The deposition rate and chemical status of deposited TiO_2 in the STO ALD change with respect to the last reactant introduced into the chamber. In particular, the TiO_2 deposited when the SrO ALD was performed with H_2O as the reactant instead of O_3 had more defects than that from SrO ALD with O_3 [Fig. 13(a)]. Even though the deposited TiO_2 had more defects, the final STO thin film exhibited significant crystallinity enhancement [Figs. 13(b)–13(d)]. Eventually, a remarkable dielectric constant of 236 was achieved [Fig. 13(c)], which is the highest value of STO thin films deposited by ALD. It seems that the unstable phase in TiO_2 had a relatively higher energy level than that of the stoichiometric TiO_2 phase, making it easier to overcome the energy barriers to atom movement of Sr, Ti, and O to the perovskite crystal structure positions. In this result, the defective phase in the STO thin film was rather beneficial and enhanced the crystallinity of the STO film. Namely, the imperfect ALD subcycle induced significant improvements in ternary oxide ALD.

Dead-layer effect

Even if the crystallinity of the insulator is perfect, the measured capacitance value in the actual device is less than the expected or calculated value. Among many factors that can be involved in capacitance degradation in an actual device, the most severe is the dead-layer effect. The dead-layer effect includes all the effects that reduce the capacitance of the MIM structure in the interfacial region of the insulator and metal electrode; indeed, "dead-layer" indicates the degraded interfacial region. Many mechanisms have been suggested for dead-layer effects. Among them, one of the widely accepted mechanisms is the E-field screening capability of the metal electrode intrinsically would govern the dead-layer effect [88, 89]. Some applied E-fields will penetrate into the metal electrode because of poor E-field screening of the metal electrode, resulting in a decrease in effective E-fields applied on the insulator layer. In this regard, noble metals such as Pt can reduce the dead-layer effect based on their higher E-field screening capability. However, in an actual case, using a noble metal as the electrode does not improve the capacitance density of the MIM structure compared with conventional electrode materials such as TiN, or Ru [34, 90, 91, 92]. Hence, practical aspects, such as crystallinity degradation at the interface, would be more important for improving the total capacitance of an MIM structure by reducing the dead-layer effect. Therefore, several results dealing with the dead-layer effect based on the nature of the interface between the insulator and electrode have been reported.

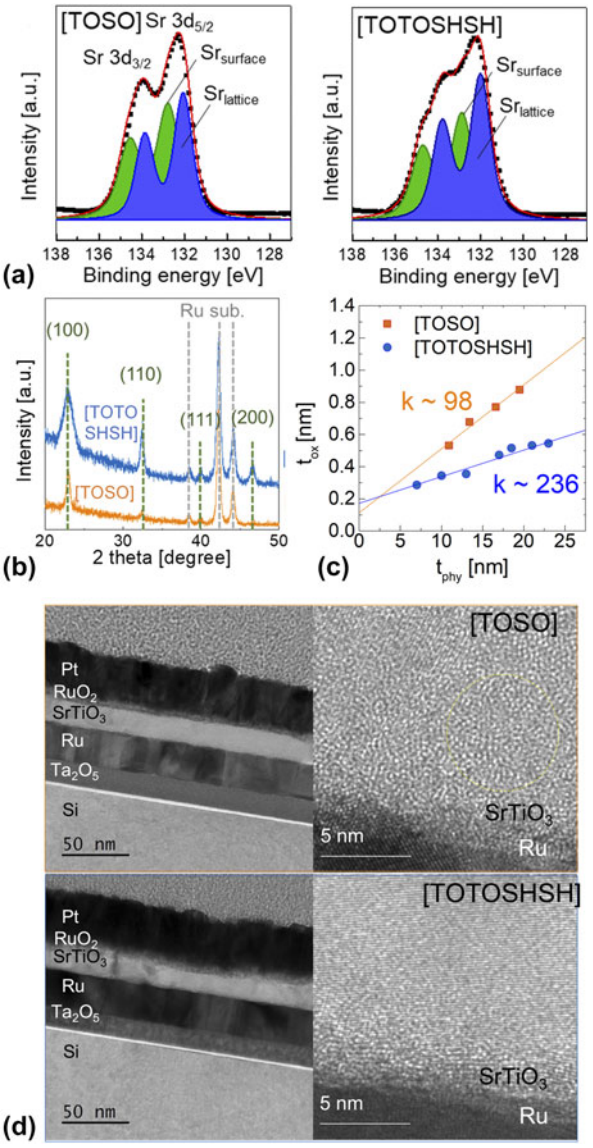

Figure 13: (a) Peak fits of Ti 2*p* spectra of STO films deposited by (left) [TOSO] and (right) [TOTOSHSH]. (b) XRD spectra of the STO films deposited by [TOTOSHSH] (H_2O) and [TOSO] (O_3) sequences. (c) Variation of equivalent oxide thickness as a function of the physical thickness of STO films with the STO films deposited by [TOSO] and [TOTOSHSH] sequences. (d) Cross-sectional image of the MIM structure consisted with STO, and (right) magnified image of the STO film right above the bottom Ru electrode [Reprinted with permission from Ref. 87. Copyright (2018) American Chemical Society].

Dead-layer effect by crystallinity degradation of the insulator at the interface

As mentioned earlier, use of noble metals as electrodes has attracted a lot of attention to enhance the performance of MIM structures. This is attributed to the advantageous electrical properties of the noble metals, including effective E-field screening and a higher work-function. Pt metal has the highest work-function value among noble metals, and it has been used as a metal electrode to reduce leakage current in the MIM structure. However, there have been no results about

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experimentally demonstrating capacitance density improvements in actual MIM structures by adopting noble metal electrodes [34, 90, 91, 92]. In contrast to the theoretical results [88], the capacitance density of the MIM structure with the noble metal decreased compared with that of a metal that has lower E-field screening capability. These results imply that there is another dominant factor in the capacitance density degradation by the dead-layer effect.

To clarify this factor, changes in the electrical properties of the top electrode of an MIM structure were investigated for devices in which ATO was the insulator layer [92]. In this study, RuO_2 and Pt were used as top electrodes because they have quite different intrinsic natures, sufficient difference in work-function (~0.8 eV), and are representative of conductive oxides and noble metals, respectively. Although Pt seems preferable to eliminate the dead-layer effect from its beneficial intrinsic properties compared with that of RuO_2, the measured capacitance density value indicates that a RuO_2 top electrode is favorable to enhance the capacitance density value of the MIM structure [Fig. 14(A)]. In the as-deposited state, the capacitance density of an MIM capacitor with a RuO_2 top electrode exhibited a slightly higher value of ~10% than that having a Pt top electrode. However, after the PMA process, the difference in capacitance density between RuO_2 and Pt top electrodes significantly increased to ~38%. During these processes, the bulk dielectric constant of Al-doped TiO_2 [as calculated from slope of the equivalent oxide thickness (t_{ox}) versus physical oxide thickness (t_{phy}) curve] was identical for all samples with various thicknesses. This indicates that the difference with respect to the top electrode is solely caused by a change at the interfacial layer of the dielectric and electrode, which is called the "dead-layer." Accordingly, transmission electron microscopic (TEM) analysis was performed to determine the difference at the interface [Fig. 14(B)], which induces differences in capacitance density. TEM analysis showed significant differences in crystallinity of the ATO film at the interface depending on the top electrode material. When Pt was used as the top electrode, an amorphous region in the ATO film was clearly observed at the interface with Pt. By contrast, the Al-doped TiO_2 film had a perfectly crystalline structure (even at the interface) when RuO_2 was adopted as the top electrode. This difference originated from the crystal structure coherence of the dielectric and electrode. RuO_2 has a common crystal structure with the TiO_2 rutile phase, resulting in recrystallization of the interfacial region of Al-doped TiO_2. However, Pt does not have any crystal structures in common with Al-doped TiO_2, which resulted in severe degradation of the crystallinity of Al-doped TiO_2 located at the

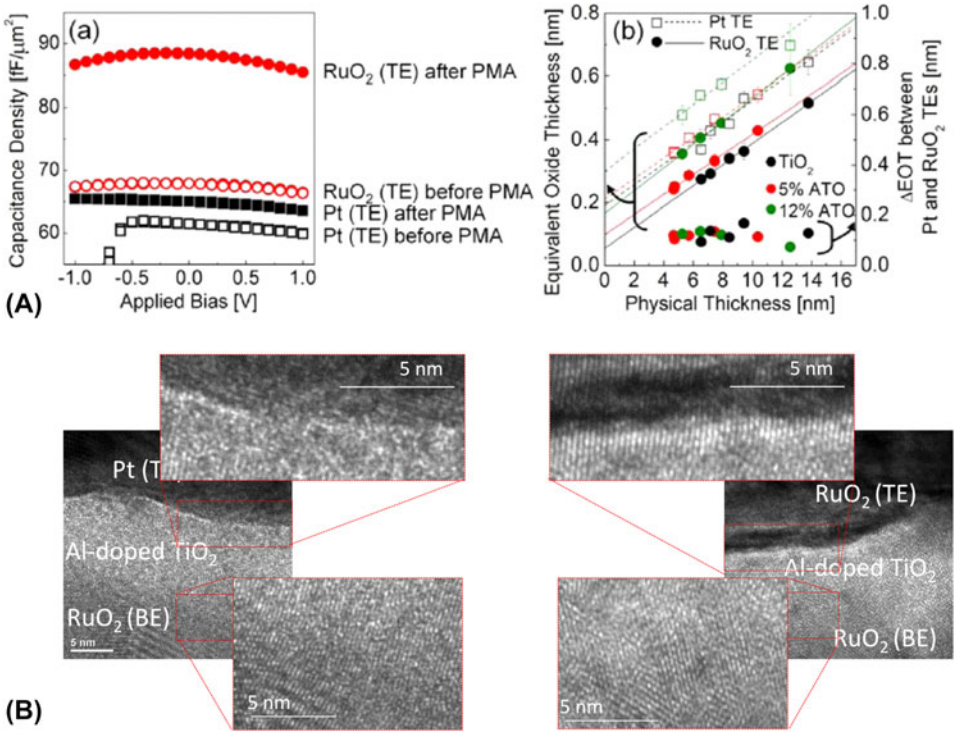

Figure 14: (A) (a) Difference in the *C–V* curve of the 9.5 nm thick ATO film (5% Al) deposited on RuO_2 with respect to RuO_2 (red) and Pt (black) TE, and before (open) and after (closed) the PMA process. (b) t_{ox} (left axis) versus t_{phy} of the TiO_2 and ATO films for RuO_2 (closed) and Pt (open) TE, and EOT difference (right axis) between Pt and RuO_2 TE for each TiO_2 and ATO film. (B) Cross-sectional TEM images of the MIM structure with (left) Pt and (right) RuO_2 top electrode. [Reprinted with permission from Ref. 92. Copyright (2014) American Chemical Society.]

interface. Therefore, the difference in coherency of the crystallinity of electrodes with dielectric films caused differences in crystallinity of the dielectric film in the interface region. This is because the difference in t_{ox} of the MIM structure as a function of t_{phy} of the dielectric film was constant regardless of the t_{phy}. The y-intercept in t_{ox}–t_{phy} plots for RuO_2 and Pt top electrode samples showed the same difference for changes in t_{ox}. This implies that enhancements caused by a RuO_2 TE solely originate from improvements in the interface region. In other words, capacitance degradation originated from the interface of the insulator, and the electrode was successfully improved by inducing recrystallization of the amorphized region of an insulator at the interface by adopting an electrode that had a crystal structure similar to that of the insulator. Consequently, the factor that most strongly influences the dead-layer effect is degradation of crystallinity of the insulator at the interface with the electrode. The crystallinity coherency between the insulator and electrode can successfully suppress the dead-layer effect.

In the same manner, an MIM structure with ZrO_2 as an insulator also showed a change in capacitance density based on the electrode material [34]. When TiN was used as the electrode, the device suffered from leakage current degradation caused by the formation of TiON at the interface. Even so, the capacitance density of the MIM structure exhibited the highest value when TiN was used as the electrode compared with other electrode materials such as RuO_2 and Pt. TiN has only one advantage over the other materials, namely, crystallinity coherence. Among the various electrode materials examined in this result, such as TiN, RuO_2, and Pt, TiN has the most similar crystal structure with a small lattice mismatch of *xx* %. This influences the dead-layer effect and overcomes the advantages provided by other electrode materials (i.e., E-field screening or robustness to chemical reaction). This is because the TiN has been used as the electrode for the MIM structure with ZrO_2 as an insulator [93, 94, 95, 96]. Thus, crystallinity coherence is the most important aspect for the dead-layer effect in MIM structures.

Summary

Two strategies were considered for increasing capacitance density of the MIM structure: enhancing the crystallinity of the dielectric and managing the interfacial dead-layer. However, these two strategies are intrinsically the same because the dead layer is reflected in the crystallinity degradation of the dielectric at the interface with the electrode. In other words, enhancing the crystallinity of the dielectric layer is the only way to effectively increase capacitance density. In this regard, various methods have been suggested to obtain the desired crystal structure and enhance the crystallinity of the dielectric. Exploiting the dopant has been suggested for obtaining a specific crystal structure with a relatively higher dielectric constant than the others. Generally, dopants in a dielectric deteriorate the crystallinity of the dielectric. However, selected dopants and optimized concentrations induce crystallization to other crystal structures that are generally not in the most stable phase because of induced internal stress. The dopant is simultaneously used in the dielectric to reduce the leakage current. Therefore, introducing the dopant in the dielectric is a general approach for enhancing the properties of an MIM structure.

Conclusion

Physical and chemical mechanisms involved in the change in leakage current and capacitance density, which are the most crucial properties governing DRAM operation characteristics, were revealed in a comprehensive discussion of previously reported results. The most important thing for enhancing leakage current properties is determining the carrier conduction mechanism in the operation voltage region of the device, followed by investigating effective solutions for reducing leakage current based on the appropriate carrier conduction mechanism. Capacitance density depends on crystallinity of the dielectric, and the crystallinity coherence between dielectric and electrode becomes more important as the proportion of interface increases. The conclusions revealed in this review may pave the way for efficient and effective development of next-generation DRAM capacitor materials and processes.

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