

## Characterization of Nanoscale Lattice Strains in Si CMOS By Convergent Beam Electron Diffraction (CBED)

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One of the major issues of concern with the scaling down of the IC size is the stress built up in the active layers of advanced Si CMOS devices, which affects the device performance [1]. Conventional lattice strain measurements using micro-Raman spectroscopy [2] or x-ray diffraction [3] could not be used due to the lack of spatial resolution needed for the characterization of nanoscale devices. The TEM/CBED method is a powerful method for measuring local lattice strains due to its high spatial resolution and sensitivity. In this paper, we present results on the nanoscale local lattice strains measured from a Si PMOS transistor at a 37 nm gate length.

A recessed SiGe epitaxial layer was used to compressively strain the PMOS. A detailed process flow is described elsewhere [4]. Fig. 1 is a cross-sectional TEM image, showing a 37nm gate PMOS with SiGe integrated at the drain extension (DE). This local strain approach is expected to improve the hole mobility. Site-specific TEM samples were prepared by FIB. The thickness of the TEM sample chosen for CBED analysis at 200 kV was approximately 200 nm. Low power plasma cleaning was applied to remove the surface contamination. A JEMS software package was used to simulate High Order Laue Zone (HOLZ) line patterns [5].

The CBED patterns were taken in the  $\langle 230 \rangle$  zone axis (which is  $11.3^\circ$  off the  $\langle 110 \rangle$  orientation) at 200 kV from the locations marked in Fig. 1(a). Fig. 1(b) is a CBED pattern taken from a region of the sample which is unstrained. The "effective" voltage was found by comparing the experimental and simulated ones. This "effective" voltage, which was found to be 200.37 kV, was used to analyze the patterns taken from the strained region (Fig. 1(c)). A compressive strain of approximately 0.209% was found in this region, as expected in this device. However, the accuracy of the measurements suffered from the blurring of the pattern. This can be attributed to the non-homogeneous strain in the analyzed volume, the surface relaxation, or the thermal diffuse scattering. A Gatan Imaging Filter (GIF) was used to improve the quality of CBED patterns. Fig. 2 shows room temperature energy-filtered CBED patterns. The improvements due to energy-filtering are clearly observed. A new set of CBED patterns (energy-filtered) was taken from the locations marked in Fig. 1(a). The strain analysis indicated a compressive strain gradient that decays from the center channel region, as predicted by ANSYS based stress simulations. In conclusion, we have successfully analyzed local lattice strains by CBED from the channel regions in a Si CMOS device with a gate length as small as 37 nm. A new choice of zone axis such as  $\langle 560 \rangle$ , which is  $5.2^\circ$  off the  $\langle 110 \rangle$  orientation, is also being explored in order to minimize the specimen-tilt projection effect, and the results will be discussed [6].

### References

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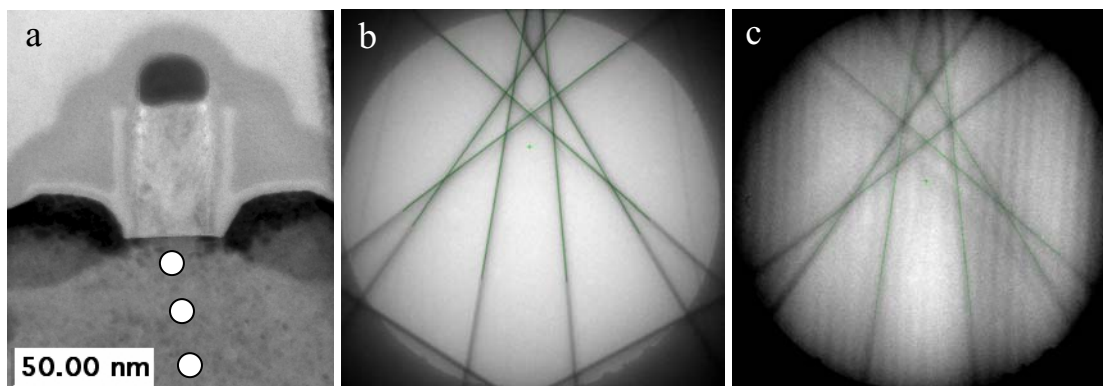


FIG. 1. (a) Cross-sectional TEM image of a Si PMOS transistor at a 37 nm gate length with SiGe layer in the DE region. Experimental  $\langle 230 \rangle$  Z.A. CBED patterns were taken from (b) the unstrained Si and (c) the region under the channel, superimposed by simulated patterns. The strain analysis indicates a compressive strain of approximately 0.239%.

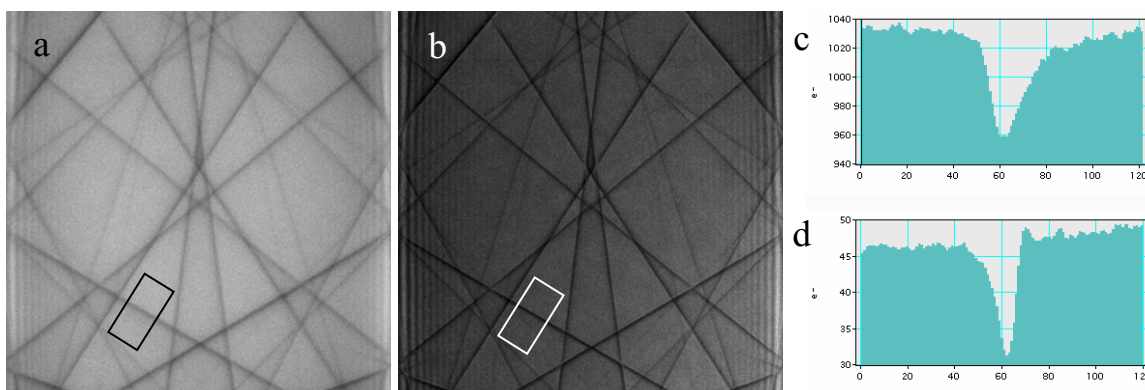


FIG. 2. Experimental  $\langle 230 \rangle$  CBED patterns: (a) unfiltered and (b) energy-filtered. Intensity line scans across the marked areas in (a) and (b) are shown in (c) and (d), respectively. Note the narrow line profile in the filtered one (d).

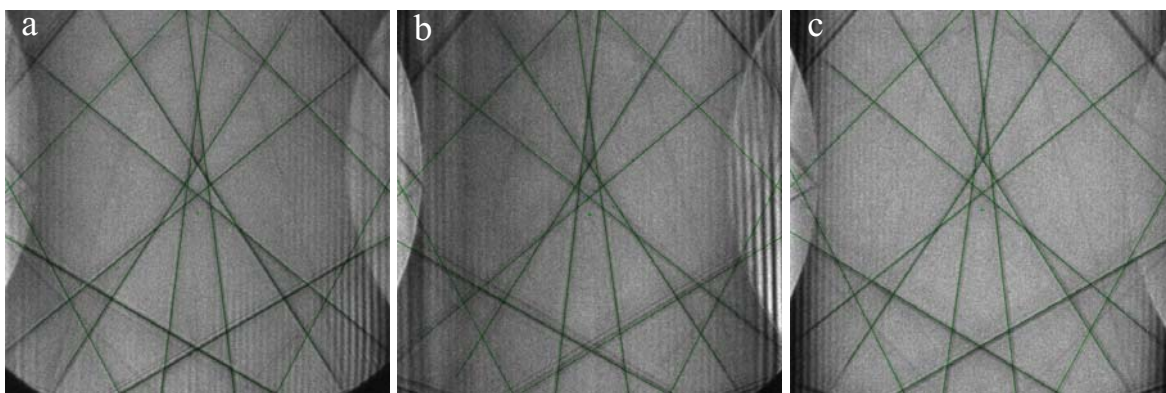


FIG. 3. Experimental  $\langle 230 \rangle$  CBED patterns taken from the regions shown in Fig. 1(a), superimposed by simulated ones. The strain analysis indicates a compressive strain gradient that decays from the center channel region: (a) 0.276%, (b) 0.203%, and (c) 0.129%.