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High-accuracy electron tomography of semiconductor devices.

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As semiconductor industries have implemented three dimensional (3-D) structures in order to improve device performance, i.e., to decrease power requirement and to lower current leakage, a conventional 2-D TEM cross-section is no longer sufficient to visualize the structure of a device. Electron Tomography (ET) provides more comprehensive representation in comparison to conventional 2-D cross section TEM images. Electron tomography allows for object visualization of practical interest at sub-nm resolution in 3D. For undistorted rendering and accurate measurement of object dimensions the data must be acquired over the entire ±90° tilt range and the accuracy of the alignment of the projected images must be better than the desired resolution of the reconstructed volume [1]. Here we discuss high resolution ET investigation of semiconductor devices using nano-dot fiducial markers on samples without a missing wedge.

Figure 1 shows a) conventional cross sectional image, and b) a projected image of a rod-shaped sample from a 22-nm node computer processor chip. Answering the engineering questions requires high resolution reconstruction of a volume ~ $(150\ nm)^3$. The large investigated volume and the nature of the sample implicates that atomic column tomography is not suitable approach, but measurements need to be performed at nearly atomic resolution, i.e. well below 1 nm. The sample in Fig. 1b is composed of (from top) the circuit layer and the support silicon wafer with fiducial markers. The nano-dot fiducial markers for accurate alignment were fabricated using an electron beam induced deposition of tungsten in an SEM [1] The images were acquired in a TEM mode of a Hitachi HF-3300 TEM operated at 300 keV. The tilt range was ±90° with 3° step. Collection semiangle of ~100 mrad was used to reduce the effect of diffraction contrast [2]. The accuracy of the alignment using the nano-dot fiducial markers is less than 1.9 pixels RMS at 0.67 nm/pix. Filtered back projection was used to reconstruct the 3D volume.

Figure 2-4 shows slices extracted from the reconstruction. Three PMOS tri-gate transistors with tungsten contact to the Si-fin can be seen in Figure 2. The corners of Si-Ge diamond were etched between adjacent cells, eliminating a short between neighboring transistors as shown in fig. 3. Figure 4 shows section along lines A, B and C indicated in Figure 2.

In summary, the current generation of computer processor chips was imaged by electron tomography utilizing rod-shaped sample without a missing wedge. Using fabricated nano-dot fiducial markers allowed to clearly image features within sub-10 nm objects. As more and more devices move from planar to 3-D design structure, for instance flash memory devices [3], electron tomography will become essential to provide a comprehensive structural representation of these innovative breakthroughs [4].

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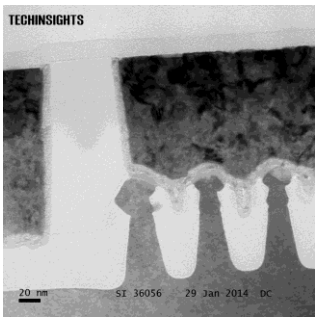

Figure 1 cross sectional TEM image of 22 nm node computer processor chip.

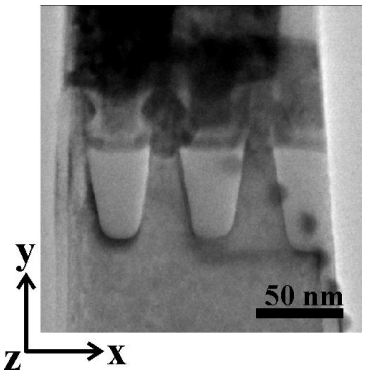

Figure 1 b) projected image from a tilt series of 22 nm node processor chip. It shows the carbon layer with fiducial markers, device layer and the Si wafer.

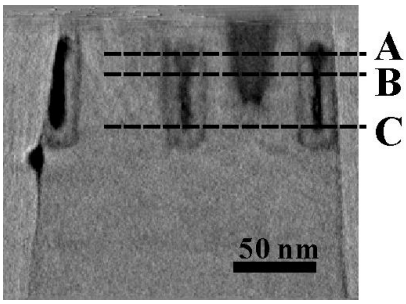

Figure 2 X-slice showing Si-Ge diamond shape under tungsten contact right on top of the fin.

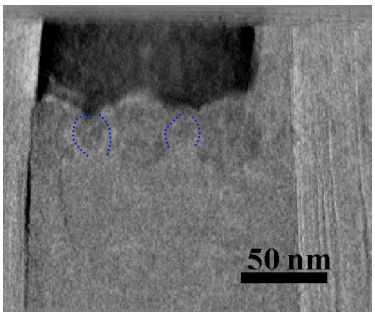

Figure 3 Z-slice showing three PMOS transistors with one tungsten contact to Si-fin.

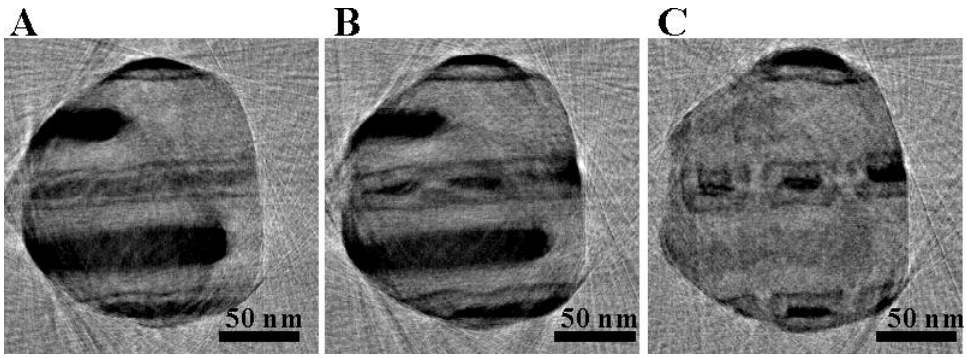

Figure 4 Y-slice images of the gate along the sections indicated in Figure 3.

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