applied, the induced torque causes the pieces to rotate out of the plane on tiny hinges and lock into place.

Chang Liu, a professor of electrical and computer engineering and director of the Micro Actuators, Sensors, and Systems Laboratory at UIUC, said, "By varying the amount of magnetic material attached to the flaps, we can control the speed at which the parts fold into position. This creates a sequential assembly process that can significantly improve the speed and efficiency of fabricating large arrays of 3D structures."

Magnetic actuation could be used to create arrays of neural probes, micro-optical devices, or miniature testing devices for integrated circuits, Liu said. The fabrication process also makes possible the development of a modular building block for the construction of a new class of integrated microsensors.

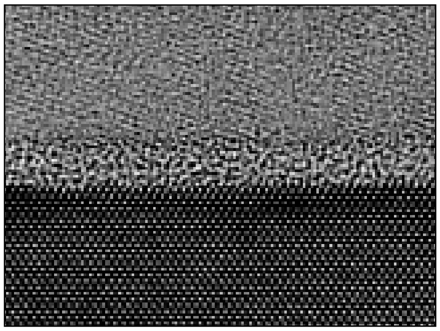
Liu has recently teamed up with UIUC entomologist and neurobiologist Fred Delcomyn to develop a microintegrated sensor that mimics the action of a hair cell. "The hair cell is a very fundamental structure consisting of a long cilia attached to a neuron," Liu said. "Nature uses this basic building block in a variety of ways to accomplish such sensing tasks as hearing, balance, and touch."

The use of microelectromechanical fabrication techniques offers opportunities for creating artificial hair cells with a size scale and frequency response comparable to their biological counterparts, Liu said. The resulting sensors could be used in many applications, including autonomous robots that more fully perceive and respond to their environment.

Liu presented this work at the NASA Nanospace 2000 meeting in January, and will present related work at the World Congress on Medical Physics and Biomedical Engineering, July 23–28 in Chicago, and at an IEEE meeting in October in Arizona.

Reliable 1.6-nm Gate Oxides Produced

Silicon chips may reach their performance limits several years later than previous predictions, according to researchers at Lucent Technologies / Bell Labs. A limiting factor in producing increasingly smaller and faster silicon-based transistors is the transistor's insulating layer. Made of silicon dioxide, the insulating layer on chips currently averages 12 atomic layers thick. While various research groups have said that 9–10 atoms would be the thinnest insulating layer for reliable, practical silicon chips, Ashraful Alam of Lucent Technologies / Bell Labs and his colleagues have shown that the intrinsic reliability limit is fewer than six atoms, or 1.5 nm. As a result, the researchers concluded that the "doomsday" scenario for the conventional silicon chip might be delayed until after 2005, instead of the next couple of years, as had been predicted.



High-resolution transmission electron microscopy image showing a 1.6-nm gate oxide. (Credit: Frieder Baumann, Lucent Technologies/Bell Labs.)

The insulating layer, also known as the gate oxide, is the device's smallest feature. It lies between the transistor's gate electrode, which turns current flow on and off, and the channel through which this current flows. The gate oxide acts as an insulator by protecting the channel from the gate electrode, thus preventing a short circuit.

To obtain their reliability results, the researchers first studied how thicker gate-oxide layers withstand high voltages over many days and developed computer models to simulate those results. They then used the same physics-based models to show that a transistor with a 1.5-nm gate oxide operating at 3 V for several hours would be comparable to a similar transistor operating at 1 V for 10 years.

As reported in April at the International Reliability Physics Symposium in San Jose, this theoretical work was confirmed by experimental work on ultrathin gate oxides. Using conventional manufacturing techniques, the research team made the ultrathin gate oxides by growing atomic layers that were exceptionally uniform and smooth (see figure). The team then tested the reliability of the transistors, verifying their theory.

Zr-Rich Pyrochlore Stabilizes Radiation Resistance

In a collaborative effort of the University of Michigan (UM), the Pacific Northwest National Laboratory (PNNL), the Australian Nuclear Science and Technology Organisation, and the Indira Gandhi Centre for Atomic Research in India, a team of researchers has found that gadolinium zirconate ($Gd_2Zr_2O_7$) resists radiation, serving as a basis for developing a very durable storage material for the safe disposal of plutonium. Lead author and UM postdoctoral fellow Shixin Wang and the research team published their results in the December 1999 issue of the *Journal of Materials Research*, and are scheduled to present their work at the Plutonium Futures 2000 Conference on July 10 in Santa Fe.

The researchers prepared pyrochlore samples from gadolinium titanate to gadolinium zirconate, varying the amounts of titanate to zirconate. When they analyzed the temperature-dependence of amorphization dose of 1 MeV Kr^+ irradiation on the $Gd_2(Zr_xTi_{1-x})_2O_7$ composition, they found an increasing resistance to radiation in response to an increase in Zr content and a decrease in temperature for amorphization. The researchers reported that for Zr-rich systems ($x = 0.5$), amorphization did not occur above 380 K.

High-resolution electron microscopy (HREM) observation revealed that $Gd_2Zr_2O_7$ transformed from a pyrochlore to a fluorite structure in response to 1 MeV Kr^+ irradiation, identical to stabilized cubic zirconia, thus stabilizing the composition's resistance to radiation. Previous studies attributed the stability of zirconate in part to the Zr–O bond. The transformation of $Gd_2Ti_2O_7$ from a crystalline structure to the fluorite structure, however, was found to be unstable relative to the amorphous state. The researchers said that regulatory requirements developed for titanate-based ceramics can be applied to the zirconate-based ceramics.

Oxide Thin Films Fabricated with Metal Alkoxides as Oxygen Sources

By using two metal compounds in which at least one is an alkoxide, scientists in the Department of Chemistry at the University of Helsinki have discovered a way of depositing metal oxide of variable thicknesses onto silicon wafers without the formation of a SiO_2 interfacial layer. In metal-oxide-semiconductor field-effect transistor (MOSFET) technology, SiO_2 is typically a part of the gate-oxide material. In the interest of reducing device size, SiO_2 presents a problem because further reduction of SiO_2 gate-layer thickness may lead to tunneling current. Gate-oxide material with higher permittivity is desired, preferably eliminating the SiO_2 interlayer at the same time.

The atomic-layer deposition (ALD) method is conventionally applied to deposit a metal-oxide layer. The scientists said that a deposition cycle consists of "exposure to a metal precursor, a purge

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period, an exposure to an oxygen precursor, and another purge period." They said that "typical metal precursors include halides, alkyls, alkoxides, and betadiketonates, whereas water, hydrogen peroxide, ozone, and molecular oxygen have been used as an oxygen source." The problem with this approach, they said, is that the thin monolayer on top offers little protection against the oxidation of Si underneath.

As reported in the April 14 issue of *Science*, the scientists' chemical ALD approach seems to eliminate the direct oxygen source. The two-metal compound in which one is an alkoxide [$M(OR)_n$, where M = metal and R = alkyl group] produces a metal-oxide depositional layer without the SiO_2 interlayer because the oxygen preferentially bonds with the metal.

The deposition of Al_2O_3 was accomplished by first etching Si with dilute HF so that native oxide could be removed. The metal-oxide compounds used for the deposition reaction were $Al(CH_3)_3$ and $Al(OCH(CH_3)_2)_3$, with the latter being the metal alkoxide. The following reaction created the top oxide layer:

$$Al(CH_3)_3 + Al(OCH(CH_3)_2)_3 \rightarrow Al_2O_3 + 3CH_3CH(CH_3)_2.$$

TEM imaging confirmed that the SiO_2 interlayer was not produced. In addition, the scientists found that the activation temperature for these deposition reactions decreased as the branching of the alkyl group increased. They found deposition at elevated temperatures to be fast, steady, and economical.

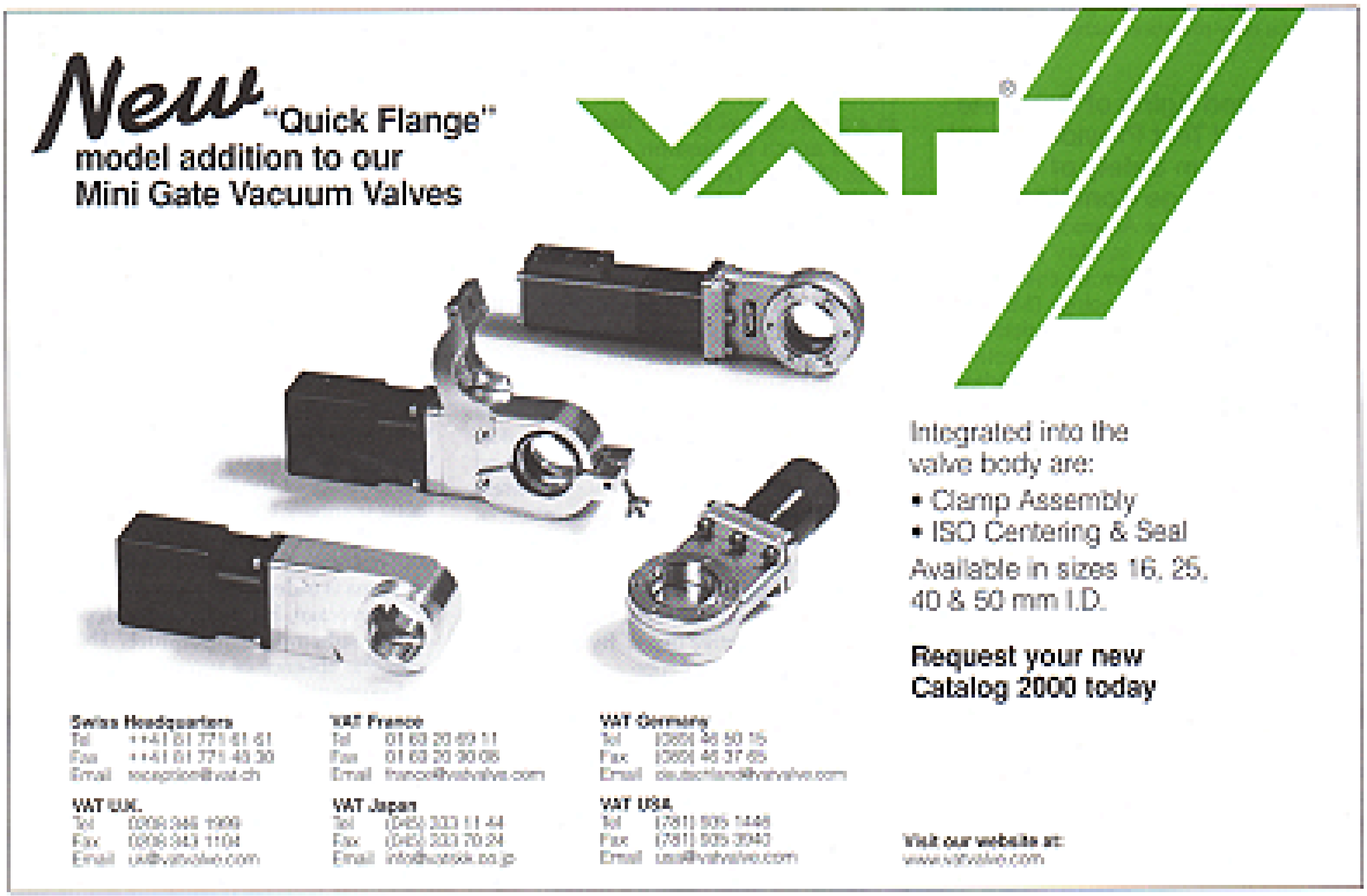
JUNE LAU

STM Utilized to Determine Structure at Atomic Scale

H.J. Lee and W. Ho at the Laboratory of Atomic and Solid-State Physics at Cornell University have accomplished molecular synthesis, bond characterization, and molecular decompilation on the atomic scale with the use of a scanning tunneling microscope (STM). Their experiments, as reported in the June 15 issue of *Physical Review B*, consist of creating and destroying bonds between copper/iron and the carbonyl $(CO)_n$ molecule(s).

Initially, a group of Cu/Fe atoms and CO molecules was scattered about on a Ag(110) substrate. The construction phase of these molecules consisted of "picking up" a CO molecule with the STM tip (at 250-mV bias and 10-nA tunneling current), positioning the tip over a Cu/Fe atom, and "letting go" of the CO molecule (with tip bias and tunneling current reduced to 70 mV and 0.1 nA). Reversing the tip bias to -70 mV and, again, increasing the tunneling current to 10 nA formed the bond between the Cu/Fe atom and the CO molecule. Additional CO molecules were attached to the Cu/Fe base in the same manner.

The first part of the characterization phase consisted of taking a topographical image of the compound. Symmetry of the CuCO molecule was noted, which suggests that the C–O bond angle is perpendicular to the substrate surface. By contrast, FeCO exhibited two distinct configurations. Asymmetry in each of these configurations suggests that the C–O bond in the Fe case deviates from the perpendicular by some angle τ. These two configurations, however, are mirror images of each other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