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Automated TEM Sample Preparation from Smaller Device Structure Regions of Semiconductor ICs using Inline Dual-Beam CLM+ and TEMLink 150

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Shrinking device features in current generation metal oxide semiconductor field effect transistor (MOSFET) structures have pushed many routine measurements and analyses beyond the resolution limit of scanning electron microscopy (SEM). Transmission electron microscopy (TEM) is a powerful tool for micro-structural analysis at high spatial resolution, but its application in the semiconductor industry has been limited in the past due to the difficulty associated with site-specific sample preparation and length of time needed to prepare samples. Recent developments in dual beam focused ion beam (FIB) based TEM sample preparation techniques have revolutionized the application of TEM in semiconductor industry [1] but faster turnaround time is the key for the success of process development, yield enhancement, manufacturing and failure analysis. High volume and fast turnaround automated inline site-specific TEM sample preparation of semiconductor ICs on 300mm wafer has been reported recently [2-4] using the dual-beam FIB/SEM system, FEI CLM+™ and TEMLink ™ 150, but its application has been limited to large device structures. This paper reports successful TEM sample preparation using CLM from smaller device structure regions. Also, the limitations of CLM based TEM sample preparation technique are discussed.

A TEM sample, in the form of a lamella, is prepared in the present work using an inline dual-beam FIB/SEM system consisting of FEI CLM+™ and TEMLink ™150. The flow of automated TEM sample preparation involves factory automation and recipe driven steps at the dual beam FIB tool and the ex-situ lift-out tool TEMLink. The main process steps in the recipe include wafer alignment, protective layer deposition, thin lamella preparation, and low kV cleaning. The typical size of the thin lamella is of the area 2.0x2.4μm^2 and thickness of 70nm that needs 25-45 min/lamella for prep and 2 min/lamella for lift-out on a TEM grid. In this work, the recipe was defined to prepare thinner ~50nm thick lamella and two challenging cases are reported based on TEM sample preparation and analysis of two smaller device regions from 20nm technology node wafers. Figure 1 (a) shows the top view SEM image containing the n-FET region (~140nm wide) for sample preparation using CLM. Fig. 1(b) shows the final sample prepared that is ready to be transferred on a 3mm TEM grid using TEMLink and Fig. 1(c) shows the TEM image confirming successful sample preparation from the n-FET structure. Another example of sample preparation and TEM analysis are demonstrated in figures 2 (a, b, c) from single contacts region, which is a much smaller (<100nm wide). Figure 2(d) is an example of clear high resolution TEM (HRTEM) image obtained from 50nm recipe from a part of figure 2(c) showing the metal gate and crossed lattice fringes in Si corresponding to d-spacing of <111> planes, indicating sample suitable for HRTEM. These examples demonstrate that CLM application can be increased by developing suitable recipes for smaller device regions. At present, the CLM based technique is limited to x-sectional sample preparation of large device structure regions due to image/pattern recognition issue and plan view TEM sample preparation is not possible, which limits its application in failure analysis [5].

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[1] Raghaw S. Rai and Swaminathan Subramanian, Journal of Progress in Crystal Growth and Characterization of Materials **55**(2009), p. 63.
[2] Hyoung H. Kang *et al*, 36th ISTFA Conference Proceedings (2010) p. 102.
[3] Roger Alvis *et al,* 38th ISTFA Conference Proceedings (2012) p. 391.
[4] Jangbae Jeon *et al,* ASM Materials Science & Technology Conference (2012), Poster # E22.
[5] The authors would like to acknowledge the TEM support from EAS TEM team of Quality - Fab8.

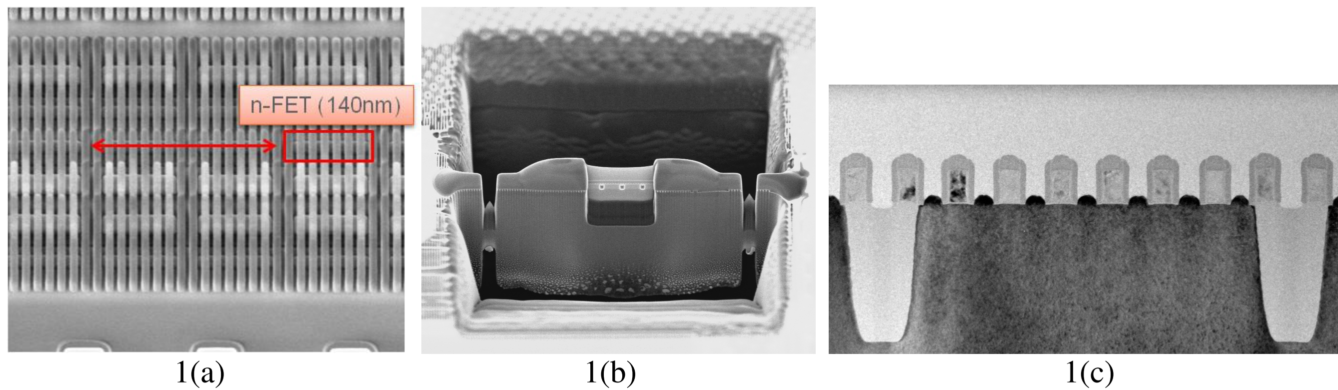

Figure 1. **(a)** shows top down SEM image containing n-FET region, **(b)** is a CLM prep TEM sample ready to be transferred to the TEM grid and **(c)** TEM image obtained from the sample confirming successful sample preparation from an n-FET structure.

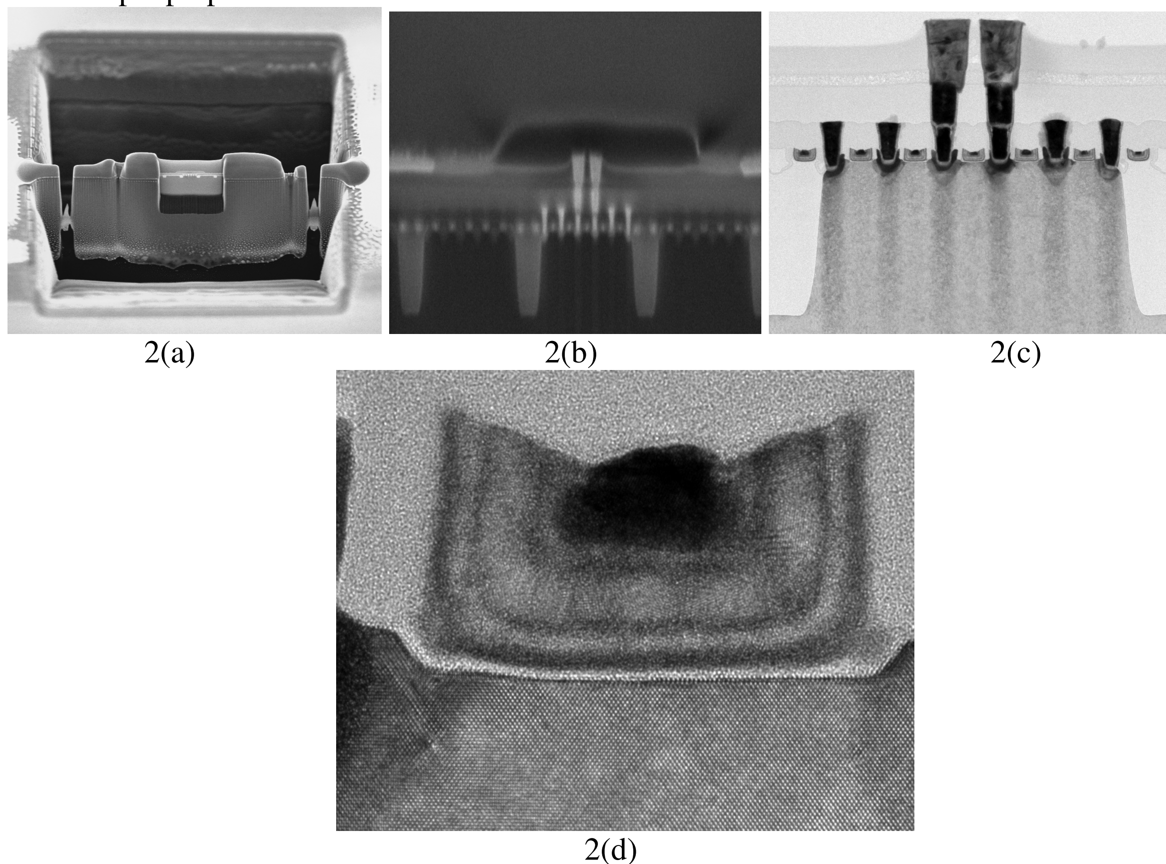

Figure 2. **(a)** CLM prepared sample ready to be transferred on the TEM grid, **(b)** X-FIB/SEM image from single contacts, **(c)** TEM image confirming single contacts region, and **(d)** Magnified image from metal gate region showing clear lattice fringes in Si, demonstrating sample thin enough for HRTEM.

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