MODELING OF A GaN BASED STATIC INDUCTION TRANSISTOR

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ABSTRACT

Static induction transistors (SITs) are short channel FET structures which are suitable for high power, high frequency and high temperature applications. GaN has particularly favorable properties for SIT operation. However, such a device has not yet been fabricated. In this paper we report simulation studies on GaN static induction transistors over a range of device structures and operating conditions. The transistor was modeled with coupled drift-diffusion and heat-flow equations. We found that the performance of the device depends sensitively on the thermal boundary conditions, as self-heating effects limit the maximum voltage swing.

INTRODUCTION

GaN is a wide-bandgap semiconductor (Eg=3.4 eV), and therefore has a high breakdown field [1] and low thermal generation rate. These properties combined with good thermal conductivity and stability make GaN an attractive material for high power/ high temperature and radiation harsh environment electronic devices. Monte Carlo simulations predict a peak electron velocity of 3.2×10^7 cm/s and a saturation electron velocity of 2.5×10^7 cm/s [2]. This makes possible high frequency operation of GaN devices.

SIT's are short channel FET structures in which the current, flowing vertically between source and drain, is controlled by the height of an electrostatically induced potential barrier under the source [3]. A cross-sectional diagram of the SIT is shown in Figure 1.

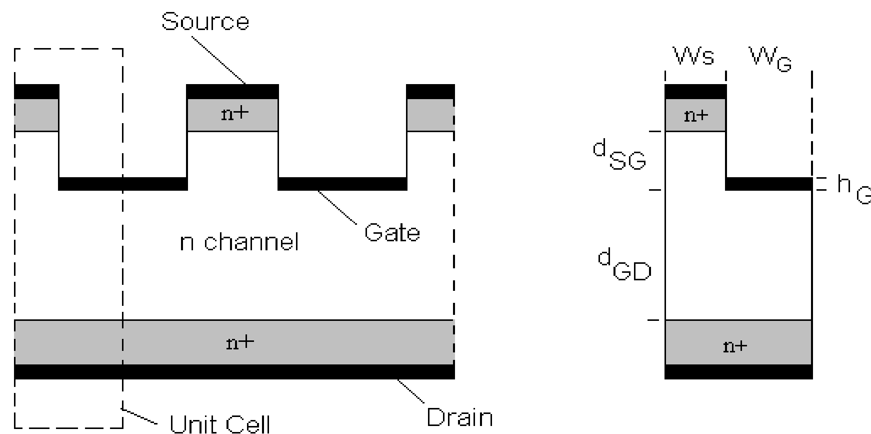

Figure 1. Cross-section of static induction transistor (SIT) structure considered in this work and the unit cell simulated with critical dimensions labeled.

Electrons are emitted from the source, which is at ground potential, and are accelerated to the drain, which is biased at positive potential, where they are collected [4]. A very thin heavily doped layer is deposited next to the drain and source contacts in order to form ohmic contacts. A grid structure is located in the space between the source and drain electrodes so the charged carriers can be externally modulated. The RF gain of the device is determined by the efficiency

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with which the modulation is affected. The grid structure is generally fabricated using pn or Schottky junctions.

A range of field effect transistors including MESFET, MISFET, inverted channel AlGaN/GaN and MODFET have been developed with potential applications for high power/ high temperature electronics [2,5-8]. To our knowledge, the highest cut-off frequency reported for GaN-based FET's is 52 GHz [9], and the maximum frequency of oscillations is over 97 GHz [10]. Significant results regarding the power output of GaN-based FET's have been reported by several groups [9, 11]. Wu reported an output power of 3 W/mm at 18 GHz, with a power added efficiency (PAE) of 19% for a 0.25 μm gate AlGaN/GaN MODFET [9]. In comparison, our SIT simulation results show a cut-off frequency f_T of 24.8 GHz, a maximum frequency of oscillations f_{max} of 75.2 GHz. Operated under class B, the output power decreases from 10.75 W/mm to 1.95 W/mm as the operating frequency changes from 2 GHz to 40 GHz. Correspondingly, the PAE changes from 73.8% to 9.1 %.

THEORY

Basic simulation equations and physical models

We employed a commercially available 2D device simulator (ATLAS [12]) which was modified appropriately for GaN, based on experimental observations and theoretical calculations. The transistor was modeled with coupled drift-diffusion and heat-flow equations. The effect of lattice temperature on the performance of the device was taken into account by including the thermoelectric factor in current density equations (1,2) and by adding the heat-flow equation (3).

$$J_n(x,y) = n(x,y)q\mu_n E(x,y) + qD_n \nabla n(x,y) - q\mu_n n(x,y)P_n(x,y)\nabla T(x,y) \tag{1}$$

$$J_p(x,y) = p(x,y)q\mu_p E(x,y) - qD_p \nabla p(x,y) - q\mu_p p(x,y)P_p(x,y)\nabla T(x,t) \tag{2}$$

$$C\frac{\partial T(x,y)}{\partial t} = \nabla(\kappa \nabla T(x,y)) + H(x,y) \tag{3}$$

where T is the lattice temperature, and P_n and P_p are thermoelectric power coefficients for electrons and holes, respectively, C is the heat capacitance per volume (1.97 J/K cm^3 [13]), κ is the thermal conductivity (1.3 W/cm K [14]) and H is the heat generation based on Joule effect.

The models used in the simulation are based on those from Si and GaAs, but have been modified to fit the available data for GaN. The temperature dependence of bandgap energy:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{4}$$

with $E_g(0)$=3.5 eV, α=9.39x10^{-4} eV/K, and β=772 K, based on optical absorption measurements [15]. The electron (hole) low-field mobility as a function of the impurity concentration (N) and temperature T is given by [12]:

$$\mu(N,T) = \mu_1 + \frac{\mu_2\left(\frac{T}{300}\right)^{\beta} - \mu_1}{1 + \left(\frac{T}{300}\right)^{\gamma}\left(\frac{N}{N_{crit}}\right)^{\delta}} \tag{5}$$

where μ_1, μ_2, β, γ, δ and N_{crit} were determined by fitting the values available from the literature for both electrons and holes [2,16-19]. For electrons: μ_1=15 cm^2/Vs, μ_2=1800 cm^2/Vs, β= -3.04,

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γ= -2.55, δ= 0.66, N_{crit}= 8x10^{16} cm^{-3}. For holes: μ_1=0.14 cm^2/Vs, μ_2=880 cm^2/Vs, β= -1.5, γ=0, δ= 0.67, N_{crit}= 5.5x10^{14} cm^{-3}. A comparison between experimental and predicted values (from Monte Carlo simulation) of low field electron mobility versus doping level and the model used in our simulations is presented in Figure 2a. Figure 2b presents a similar comparison for the electron low field mobility versus temperature [19]. In our simulations, we employ a channel doping of 5x10^{16} cm^{-3}. The low field electron mobility reported for such a doping level is 900 cm^2/Vs [5,20]. However this mobility was measured laterally. There is evidence that the lateral mobility is reduced due to the scattering by charged dislocations, while the vertical mobility is significantly higher because the electrons are repelled from the dislocation lines by band bending due to the negative charge on the dislocations [21]. In our device, which is a vertical one, we employ a room temperature electron mobility of 1050 cm^2/Vs, which we believe is a reasonable value.

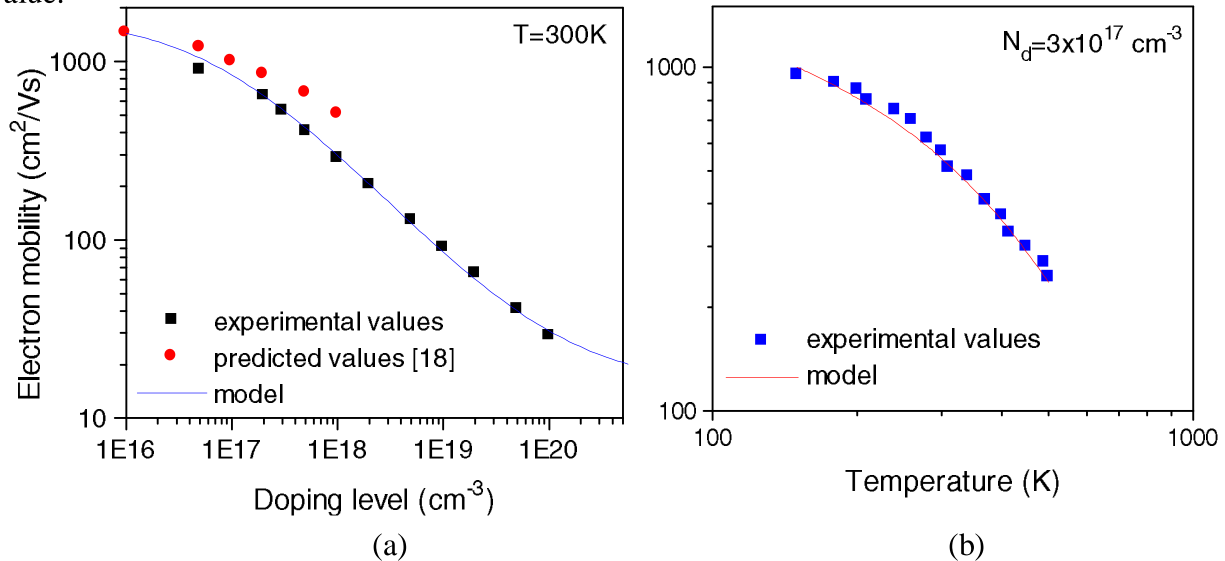

Figure 2. Electron mobility (a) versus doping level at T=300K [2, 16-19], and (b) versus temperature, for a doping level of 3x10^{17} cm^{-3} [19].

For high fields, we use a simple model for mobility versus electric field, which ignores the overshoot effect. This slightly underestimates the current, but the effect is minor for high power devices because they operate at high fields. In high electric fields, the saturation velocity is weakly dependent on temperature. The saturation velocity is modeled as a function of temperature by an empirical relation obtained by fitting the results from Monte Carlo simulation [18]:

$$v_{sat} = 2.87 \text{ x}10^7 - 9.8\text{x}10^3 \text{ x } T \text{ (cm/s)} \quad (6)$$

We assumed that optical recombination is given by:

$$R_{opt} = C_{opt}\,(np\text{-}n_i^2) \quad (7)$$

with C_{opt} =3x10^{-11}cm^3/s, from absorption experimental data and calculated electron energy band dispersion [15].

The generation rate of electron-hole pairs due to impact ionization is modeled according to Selberherr [22]:

$$G = \alpha_n \frac{/\,J_n\,/}{q} + \alpha_p \frac{/\,J_p\,/}{q} \quad (8)$$

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To our knowledge, there are no experimental measurements of impact ionization rates on GaN. However, calculations of impact ionization rates using ensemble Monte Carlo simulation including the full details of all the relevant valence bands, based on pseudopotential approach, have been published recently [23]. We assume that the impact ionization rates (α_n and α_p) are dependent on the electric field and temperature for both electrons and holes according to the formula [12, 22]:

$$\alpha(E,T) = \alpha^{\infty} \exp[-(\frac{E^{crit}}{E})^{\beta}]\{1 + A[(\frac{T}{300})^{M} - 1]\} \quad (9)$$

The critical electric field also depends on T:

$$E^{crit}(T) = E_0^{crit}\{1 + B[(\frac{T}{300})^{M} - 1]\} \quad (10)$$

By fitting the results from [23], the parameters were found to be: for electrons ($\alpha^{\infty} = 4.55 \times 10^{6}$ cm^{-1}, E_0^{crit}=1.19x10^{7}V/cm, β=1), for holes (α^{∞} = 1.48 x 10^{6} cm^{-1}, E_0^{crit}=8.95x10^{6} V/cm, β=1). Since there are no available results for T dependence of α, we use the values for silicon for both electrons and holes (A=0.588, B=0.248, M=1 [12]).

Device optimization

In order to optimize the SIT structure for operation at high power, high temperature and high frequency, DC, small signal and large signal analysis have been performed. Due to symmetry, we need to simulate only one unit cell of the transistor (Figure 1). In order to maximize the breakdown voltage as well as carrier mobility we want low doping in the channel, and 5x10^{16} cm^{-3} was chosen as a value that is achievable with current technology. As the distance between source and gate (d_{SG}) decreases, the voltage gain μ as well as transconductance, g_m increases. The value of d_{SG} is limited by the need to avoid the source to gate punch-through, when the depletion region from gate extends to that from the source. A large distance between gate and drain (d_{GD}) is desirable in order to have a large breakdown voltage. However as d_{GD} increases the series resistance also increases and this limits the frequency and current response of the device. The half-width of the source finger (W_S) determines the blocking voltage of the transistor, so it controls the voltage swing in power measurements. By balancing the above considerations we obtained the following values: the channel is 3 μm thick with a doping concentration of 5x10^{16} cm^{-3}; the n+ layers are 0.2 μm thick and have a doping concentration of 1x10^{19} cm^{-3}. The top of the device is modified in a comb configuration having the following dimensions: source half-width W_S=0.5 μm, gate half-width W_G=1.5 μm, gate height h_G=0.2 μm, d_{SG} =0.6 μm, d_{GD} =2.4 μm.

RESULTS

Our simulations indicate that the performance of the device is very sensitive to the thermal boundary conditions, as self-heating effects limit the voltage swing. In order to increase the power output we have assumed that the device is build on a SiC substrate. According to Binary [5] the SiC substrate allows about a 4x increase in power density due to the higher thermal conductivity of SiC compared to GaN or sapphire. For the same purpose, a layer of diamond paste is assumed to be present on the top of the device. We have calculated the equivalent thermal impedance of the SiC substrate and diamond layer, assuming that the length and height of the SIT is much smaller than the thickness and length of the SiC and diamond layers [12,24]. For one finger of the device, the calculations lead to a thermal impedance of 3300

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W/cm^2 K for drain contact, 12000W/cm^2 K for source contact and 4050 W/cm^2 K for gate contact. Simulated drain I-V characteristics with the gate voltages varying from 0V to -12V are shown in Figure 3a. We notice that the breakdown voltage varies with the gate bias from about 50V at 0V gate bias to 320V at –12V gate bias. The simulations indicate that the breakdown is due to self-heating effects. Our results show that the performance of the device is not significantly affected by thermal generation as long as the maximum temperature in the device does not exceed 700K. The gains obtained by small signal ac simulations for a drain bias of V_d=100V and a gate bias of V_g=-6V are plotted as a function of frequency in Figure 3b. The cut off frequency is f_T=24.8 GHz and the maximum frequency of oscillations is f_{max}=75.2 GHz.

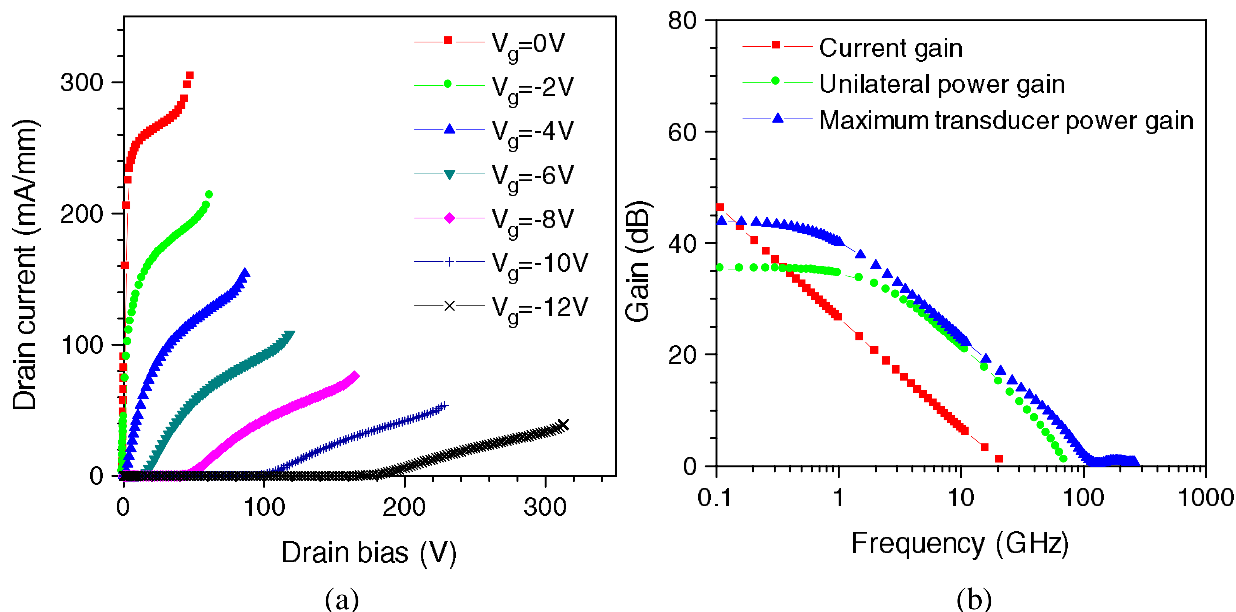

Figure 3. Transistor characteristics: (a) drain I-V characteristics, and (b) gain versus frequency. The cut-off frequency is f_T=24.8 GHz and maximum frequency of oscillations f_{max}=76.5 GHz.

Large signal analysis was performed under class B, in order to obtain the output power and power added efficiency (PAE). In Figure 4 we present the output power and PAE as functions of frequency, with a DC drain bias of V_{DD}=180V, load resistance of 7.2x10^5 ohm and a gate bias voltage swing between 0 and –12 V. Under these conditions, the output power varies from 10.75 W/mm to 1.95 W/mm and PAE varies from 73.8 % to 9.1 % as we increase the operation frequency from 2 GHz to 40 GHz. The maximum theoretical PAE for operation under class B is 78.5 % [4]. Note that operation under class B requires two transistors and gate periphery of both transistors is included in output power calculations.

CONCLUSIONS

In conclusion, we modeled a static induction transistor based on GaN films. Our results show that with a SiC substrate and top side diamond paste as thermal sinks, the output power can be as high as 10.75 W/mm at 2 GHz operating frequency, with a PAE of 73.8 %. The cut-off frequency was found to be 24.8 GHz and the maximum frequency of oscillations was 75.2 GHz. These results demonstrate the excellent potential of GaN based static induction transistors for high power, high temperature and high frequency operation.

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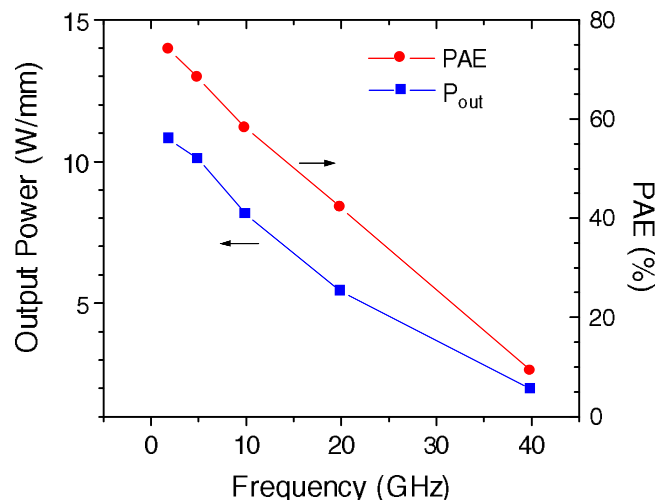

Figure 4. Output power and power added efficiency (PAE) versus frequency.

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