doi:10.1017/S1431927618005366
Microsc. Microanal. 24 (Suppl 1), 2018

Strain Characterization of Advanced CMOS Transistors: An Industry Perspective

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Moore's law is the key technological and economic driver for nanoelectronics industry. Dimensional scaling has provided performance improvement and power reduction in the era of traditional MOSFET scaling until the early 2000s, when it was realized that disruptive enhancements beyond geometric scaling would be needed. One key innovation was the introduction of strain. Strain breaks the cubic symmetry of the silicon and modifies the band structure of silicon. Large device performance gain was obtained by introducing strain in the device channel [1, 2]. Critical to the success of the development of technologies that utilize strain is the ability to analytically measure and quantify the strain. Along with the process development, significant efforts have been made in analytical techniques to support these emerging process technologies in complex patterned transistor structures containing not only Si but also Ge, III-V and other novel materials.

Transmission electron microscope (TEM) based techniques measure strain in either diffraction or imaging modes with resolution from one angstrom to a few nanometers and with good sensitivity. From Intel's 22nm process, the transistor has evolved to 3D tri-gate architecture with strain engineering from various approaches including strained epitaxial layers and stress films. The new tri-gate structure raises more challenges for strain characterization. Traditional TEM strain techniques that work for planar transistors, such as convergent beam electron diffraction and dark-field electron holography, do not apply to tri-gate transistors due to the complicated 3D tri-gate geometry. The only electron beam-based technique suitable for the tri-gate transistor is nano-beam electron diffraction (NBED) [3]. NBED separates the device channel and the overlapped materials in the diffraction patterns, as the crystalline channel gives rise to sharp Bragg diffraction spots, while the amorphous or nanocrystalline, overlapped, gates give diffuse diffraction rings and contribute to the diffraction background. The reference pattern can be collected in the same scan from the strain free substrate using NBED. Thus, NBED is the only technique capable of direct nanoscale strain measurements of the 3D tri-gate transistor. Figure 1 at the left shows the NBED line scan strain profile which is sensitive to the microstructure of the nearby epitaxial SiGe source drain. Figure 1 at the right shows the strain map of an Intel tri-gate transistor along [110] and [001] directions.

X-ray measures lattice spacing directly and nondestructively, providing a wealth of information on the composition and strain state of the probed layers and can also provide information on film defects and relaxation. X-ray has high strain sensitivity but suffers from the large spot size. Raman is another nondestructive technique with better spatial resolution than X-ray of 0.5-1.0 micron depending on the wavelength employed. Raman measures the phonon frequency shift which can be correlated with strain in the lattice. For complex 3D structures as tri-gate, modeling and simulation provide a path to extract strain values. Raman offers the benefit for die and wafer level mapping. A device-level array structures are designed to allow techniques such as X-ray and Raman to provide strain data on technologically relevant device structures. Furthermore, they can provide statistical measurements of process variations which is difficult for nanoscale TEM based methods. The concept of 'design for metrology' is a key aspect for further developing the analytical capabilities [4].

Transistor technology scaling has introduced a wider range of alternative materials and device architectures. It has been pushing strain characterization into a new era in terms of resolution, sensitivity as well as automation to provide a range of capabilities that include fundamental characterization, rapid analysis and measurements at the device, die and wafer levels. Innovative metrologies are always needed to provide a path for future strain engineering programs with a new class of emerging transistor materials and architectural options.

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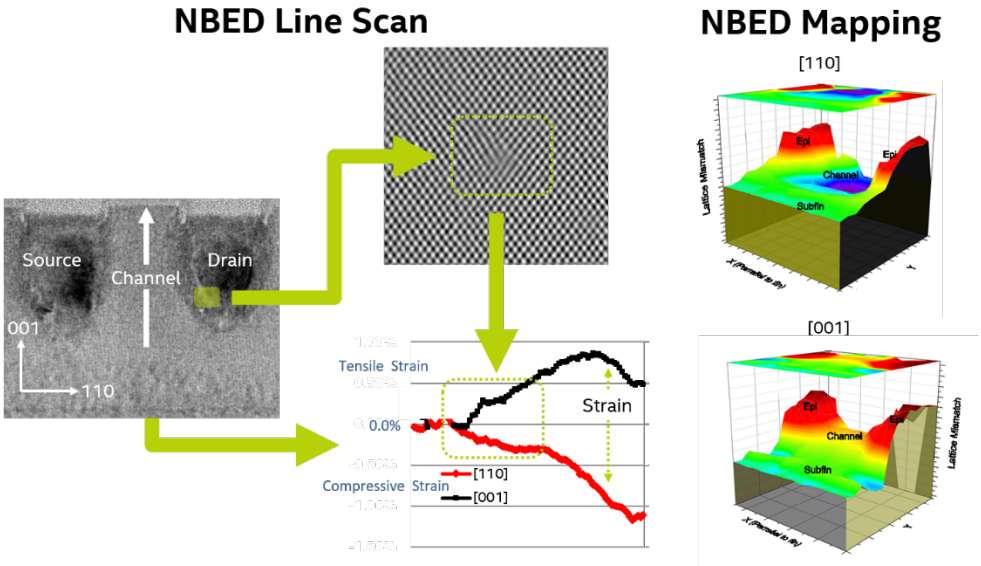

Figure 1. (Left) NBED strain line scan profile shows the strain sensitivity to nearby source/drain microstructure. (Right) NBED strain map of a tri-gate transistor in [110] channel direction and [001] direction.

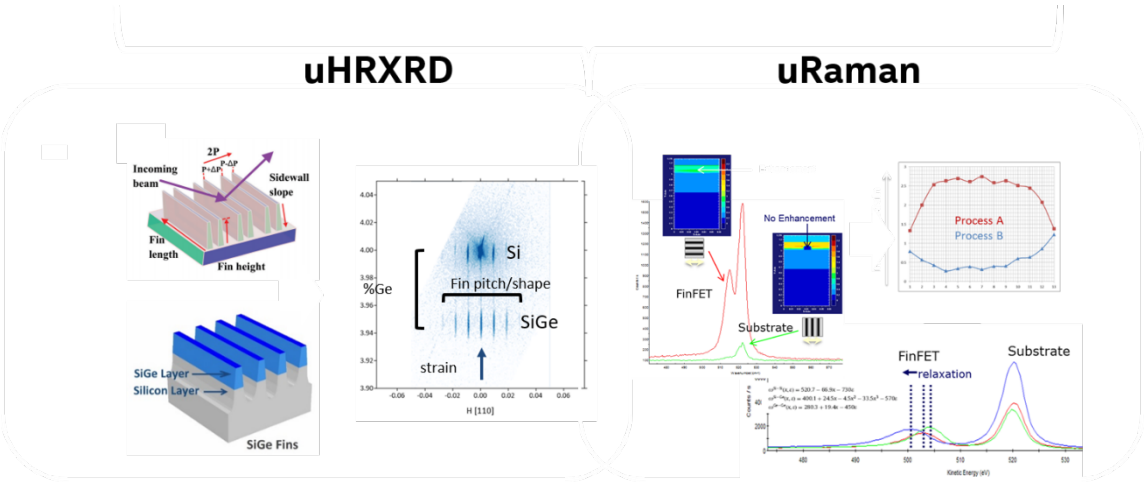

Figure 2. X-ray diffraction of tri-gate array structure (left). Raman spectroscopy (right) of tri-gate showing field enhancement effect from data and simulation and the capability of mapping the localized strain across a wafer.

https://doi.org/10.1017/S1431927618005366 Published online by Cambridge University Press