Millimeter-scale, Large Uniform Area Semiconductor Device Delayering for Physical Failure Analyses and Quality Control

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Constantly evolving microelectronic device designs continue to grow more complex, more compact, and smaller. The designs may include an increasing number of layers, three-dimensional (3D) vertical stacking, air gaps, and different material compositions. High-volume semiconductor device manufacturing requires robust quality control and failure analyses processes. Many failure analysis techniques, both nondestructive and destructive, have been developed in the past decades [1-3]. A very popular technique is device delayering, which is the controlled removal of device layers from the top-down. Information gained through this technique can support quality control, failure analyses efforts, yield product and process improvement data, as well as reverse engineering.

Conventional mechanical sample preparation is a difficult and uncontrolled process that does not allow targeting of a specific depth or layer [2, 4, 5]. Because of the difficulties presented by mechanical sample preparation, there has been an emergence of beam-based techniques for device delayering applications. Focused ion beam (FIB) technique is one of most popular used for device delayering [6, 7, 8]. However, using FIB technology for delayering has limitations; the relatively small delayering area of up to 100 x 100 μm [9-10]. Broad ion beam (BIB) milling, however, allows uniform and controlled large-area delayering that is significantly larger than 100 x 100 μm. This also allows the creation of a large slope area that exposes all of the device's layers simultaneously [11].

This paper presents a development in semiconductor device delayering by BIB milling [Model 1062 TrionMill, Fischione Instruments] that offers an effective milling area of up to 50 mm. A milling area of this size is made possible by the user's ability to position each of the tool's three ion beams individually. This flexibility in ion beam positioning also enables more precise targeting of an area of interest. The beam emission parameters can be individual adjusted for each ion source, which allows user control of beam size and beam current. The ability to fully control the delayering process is critical, especially for fully fabricated wafers, where the final aluminum pads, lines, and passivation have significant thickness. The delayering strategy can be adapted to meet the investigator's goals.

When delayering a semiconductor device, advance knowledge of the number of layers and the elemental composition and thickness of each layer is indispensable. A cross-section sample taken from the same bulk material as the sample to be delayered can yield this information and provide a roadmap for the delayering process. An example is shown in Fig. 1, which presents a SEM image of a cross-section sample and corresponding energy dispersive X-ray spectroscopy (EDS) maps. The obtained information assists in determining the optimal ion milling parameters (such as ion beam energy and milling angle) and allows better control of the delayering process.

We will show how we targeted and delayered a 2 mm diameter area, using a fully fabricated wafer that contained both logic and memory. In the example presented here, we chose to stop delayering at the top of memory cells (see the cross-section image in Fig. 1), after removing approximately 5 μm of device material, including the top thick passivation and aluminum layers.

The type of beam alignment shown in Fig. 2 was chosen for delayering. The beam energy was 6 keV (left and right beam) and 5.5 keV (center beam); the beam current and beam width were specifically tuned for each ion source. These parameters allow uniform milling over a millimeter-scale area by compensating for the ion beams continuously striking the center of the sample during stage rotation.

Figure 3a is a SEM image of the delayered area and Fig. 3b shows the quality of the sample surface after BIB milling. The delayered area is 2 mm diameter and is extremely clean and uniform. The slope area, which exposed the silicon nitrate, silicon oxide, aluminum, and copper layers, is more than 4 mm as measured from the center of the delayered area.

To quantify the uniformity of the delayered area, FIB cross-section samples were taken from different points across the milling area (see Fig. 3). The FIB cross-section samples and measurements of remaining layers thickens are shown in Fig. 4. The results show ± 130 nm uniformity of delayering across a 2 mm diameter area.

The results highlight that BIB milling produces excellent surface quality over a millimeter-scale area.
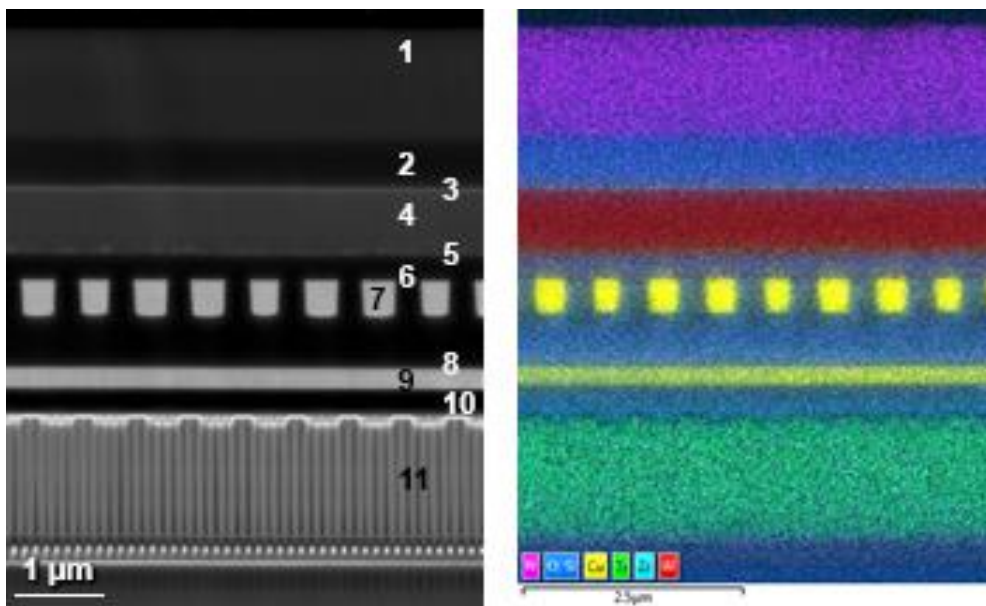

Figure 1. Cross-section sample from a device: SEM image (left) and EDS overlay maps of nitrogen, oxygen, silicon, copper, titanium, zirconium, and aluminum (right). The information gathered from the cross-section sample (number of layers, layer composition, and layer thickness) is used to inform the delayering process. EDS data collected at 10 kV acceleration voltage.
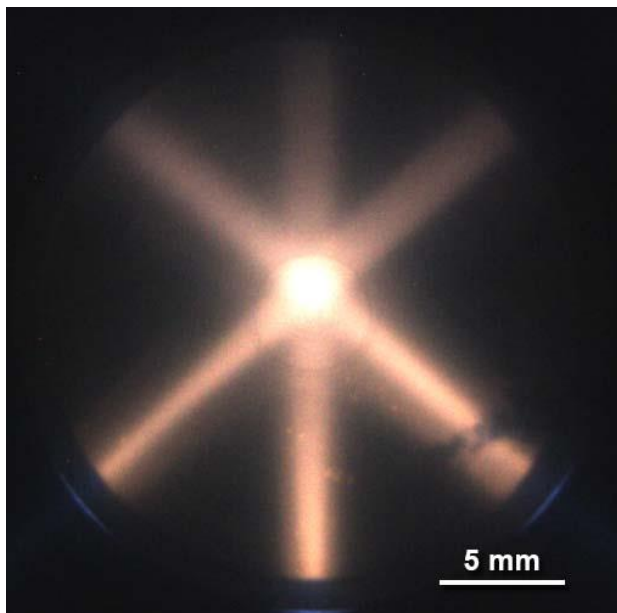
Figure 2. Image of an ion beam alignment that allows uniform milling of a large area in the Model 1062 TrionMill.
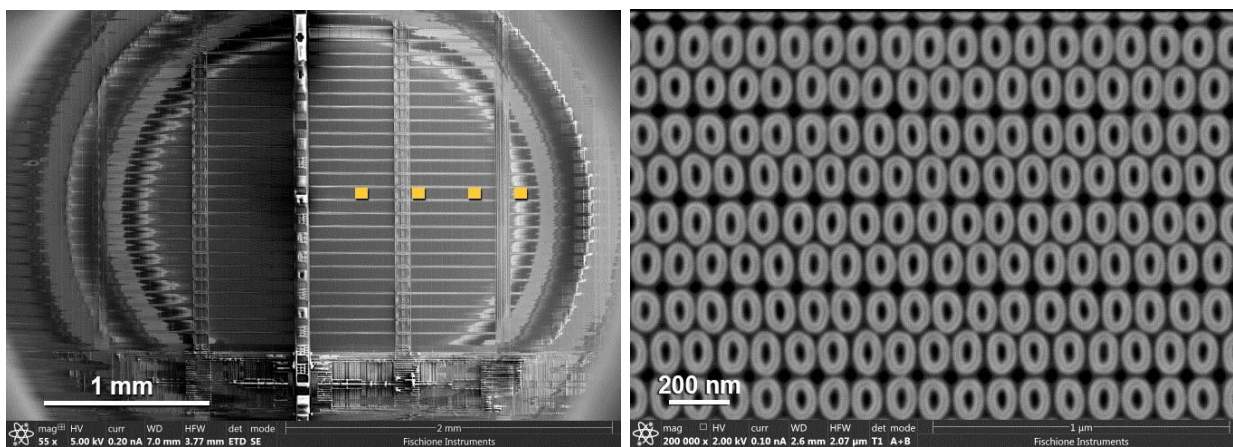

Figure 3. Device after the delayering process. (a) SEM image showing the entire delayered area; red squares indicate areas where FIB cross-section samples were taken. (b) High magnification SEM image of the top level of the memory device reveals an extremely clean and uniform surface.
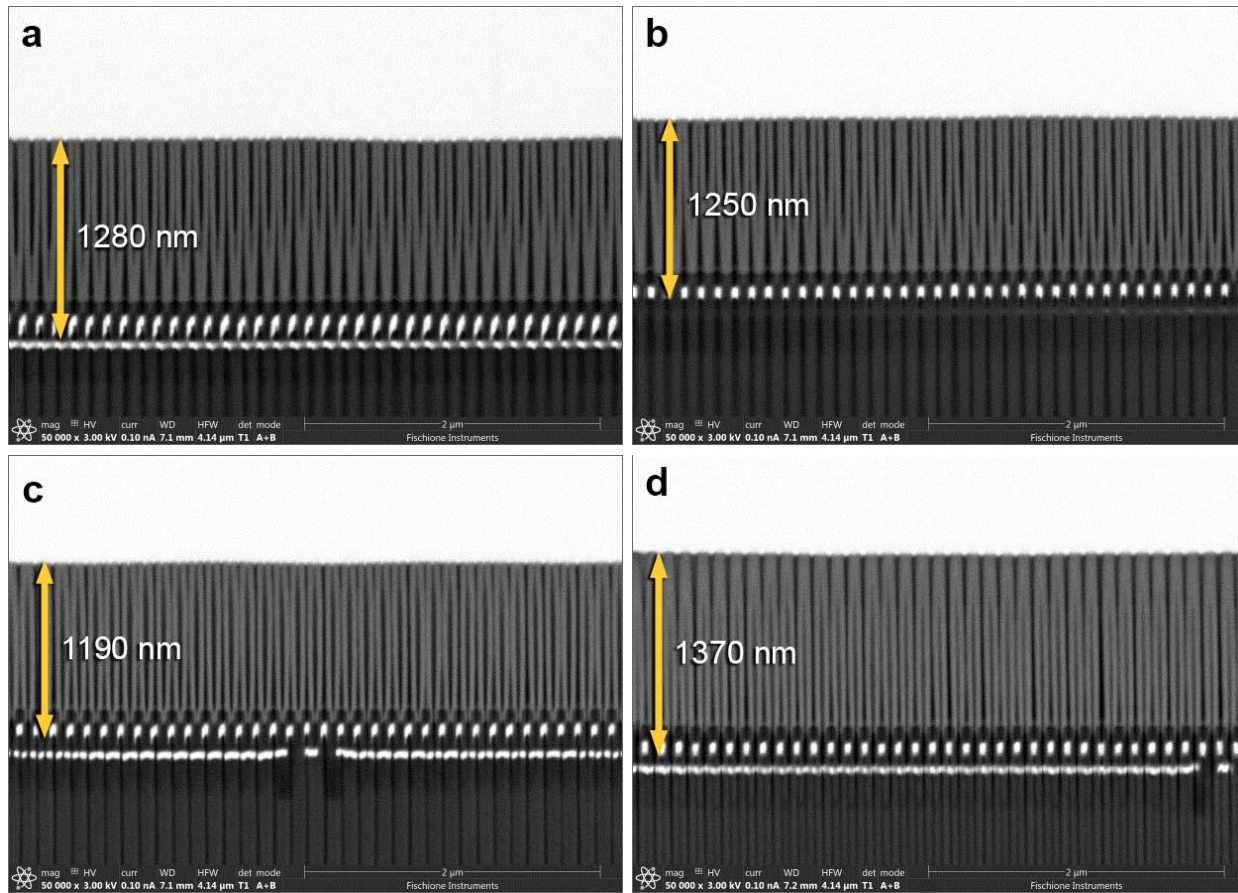
Figure 4. Cross-section samples of a delayered device prepared by FIB milling from: a) the center of the delayered area, b) 0.35 mm from the center, c) 0.7 from the center and d) the edge of the delayered area, which is 1 mm from the center. The results show ± 180 nm uniformity of delayering over a 2 mm diameter area.

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