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Moore's Law: A Review of Feature Size Shrinkage and its Effect on Microscopy in the Semiconductor Industry

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Summary: In 1965, Gordon Moore predicted that the number of components in an integrated circuit would double every year [1]. The drive for higher performance with greater economy has been a major factor in the pursuit of Moore's Law. Device scaling is expected to continue without interruption, and products manufactured using a nominal 22nm feature size should become commercially available by the year 2011. This article will detail the technology enablers that make Moore's Law possible, and the improvements in microscopy techniques required to meet the challenges that Moore's Law presents.

1. Introduction

Gordon Moore's observation of a limited data set in 1965 was not just a recognition of a technological phenomenon, it was a recognition of an economic principle. Improvements in technology made it possible to fit more transistors in less space, but the strongest motivation for doing so was economic. Failure to maximize the number of transistors per unit area would result in higher costs due to failure to take advantage of technology. However, putting too many transistors in too little space could result in too many transistors not working which would result in higher costs, since non-functional parts cannot be sold. Moore predicted an economic advantage of finding a 'sweet spot' for the pace of shrinking transistors to put more of them in less space. As the feature size shrinks, there are new demands on electron microscopy support of the new process technology.

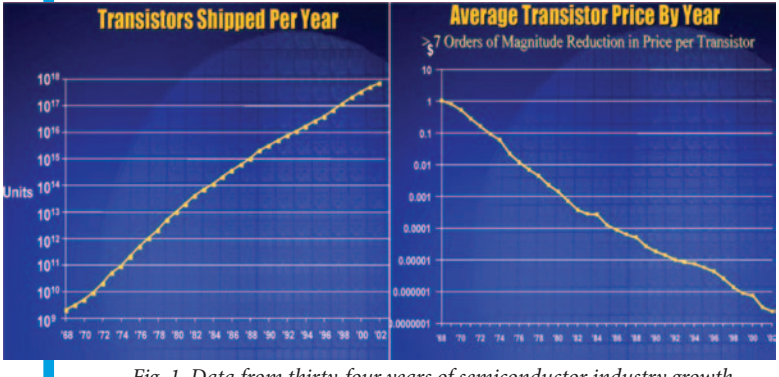


Fig. 1. Data from thirty-four years of semiconductor industry growth show nine orders of magnitude growth in the number of transistors shipped with seven orders of magnitude reduction in cost per transistor[2].

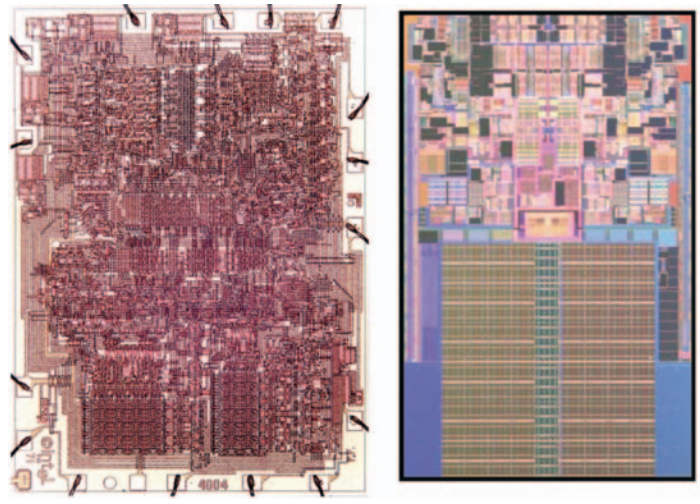


Fig. 4. Intel's first microprocessor produced in 1971 had 2,300 transistors and a gate length of 10 micrometers[2].

Fig. 5. Intel's newest microprocessor to be introduced later this year has 410 million transistors with a gate length of 25 nanometers[2].

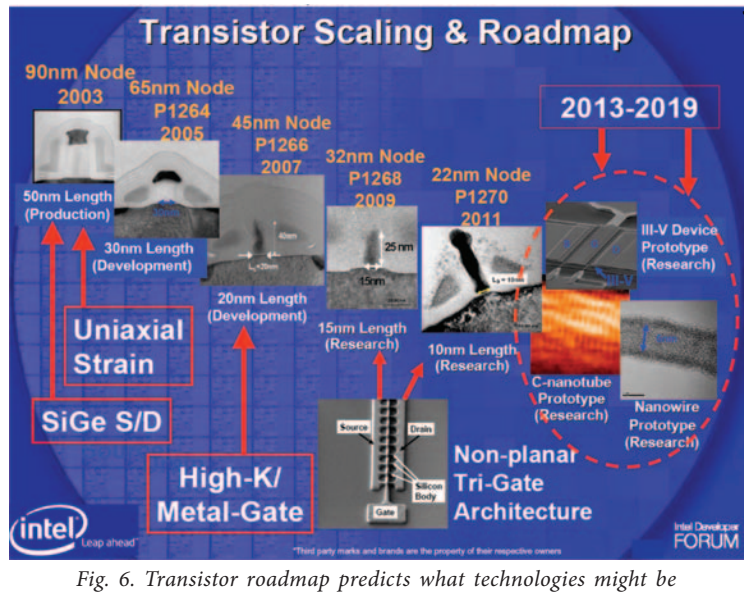
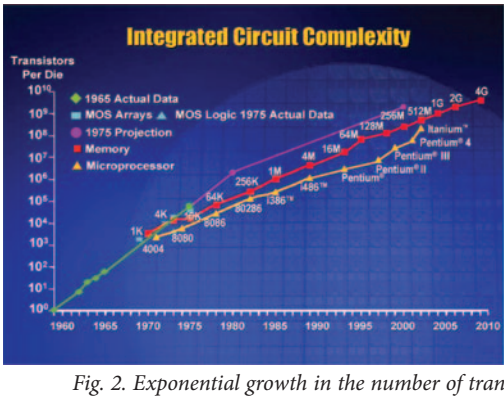


Fig. 6. Transistor roadmap predicts what technologies might be required to continue Moore's Law through the first two decades of the 21st century[2].



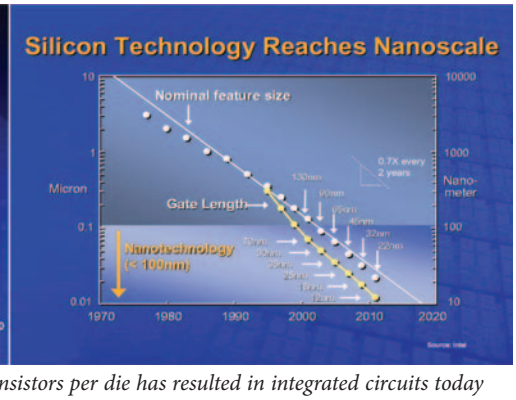


Fig. 2. Exponential growth in the number of transistors per die has resulted in integrated circuits today with over 100 million transistors[2].

Fig. 3. Exponential reduction in feature size has continued without interruption. The transistor gate length shrinkage rate has actually exceeded Moore's law[2].

2. Semiconductor Industry Growth

Moore's Law has stimulated tremendous growth in the semiconductor industry. Figure 1 shows how the number of transistors manufactured and sold each year has increased nine orders of magnitude between 1968 and 2002. At the same time, the cost per transistor has decreased nearly seven orders of magnitude, resulting in semiconductor industry revenue growth from $3 billion in 1968 to $300 billion in 2002.

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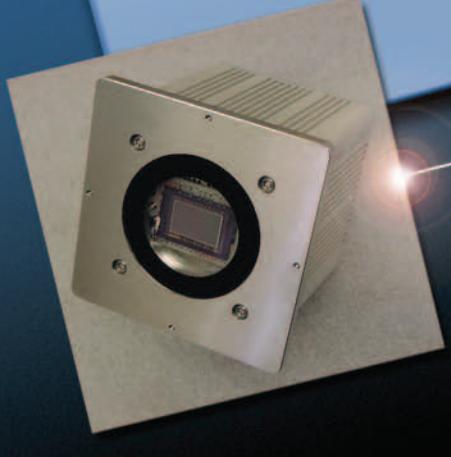

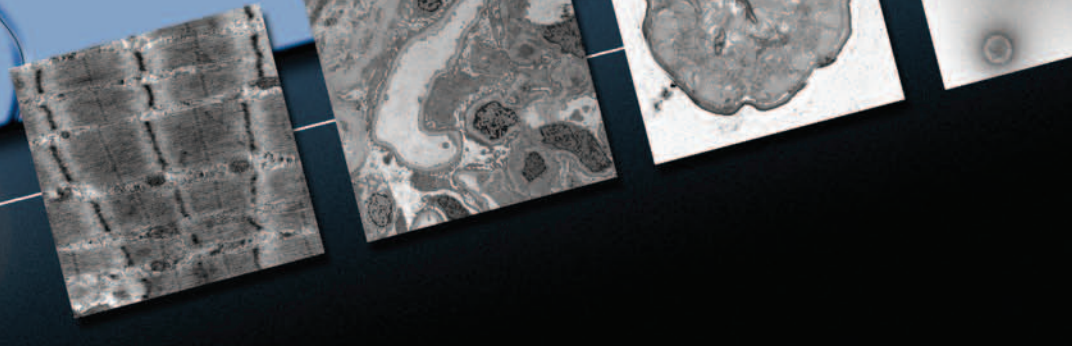

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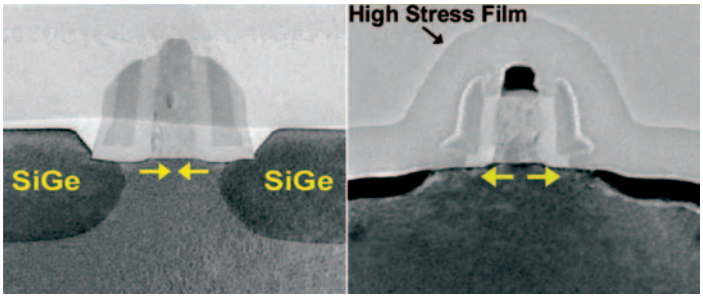

Fig. 7. Lattice strain enhances electron mobility. PMOS transistors are compressed using epitaxial SiGe[2].

Fig. 8. A stressed capping layer is used to apply tension to NMOS transistors[2].

3. Transistor Shrinkage

Moore's Law predicted in 1965 an annual doubling in the number of transistors per chip, but that was adjusted to doubling every two years in 1975. Figure 2 shows how that prediction has held true in both microprocessors and memory for over three decades. In order to accommodate the increased number of transistors, the feature size on each chip has been shrunk accordingly. Figure 3 shows how the nominal size of features has maintained a steady logarithmic shrink over three decades. The only deviation from that trend has been that the transistor gates have been shrunk even faster to produce speedier devices.

The changes in microprocessors are quite startling when the first microprocessor is compared with the latest model about to be premiered. The first microprocessor produced in 1971 had 2,300

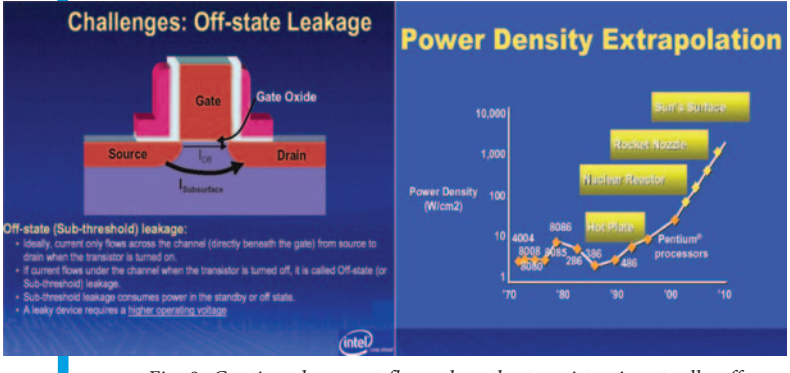

Fig. 9. Continued current flow when the transistor is actually off, combined with current leakage through the gate, wastes energy and results in excessive heat[2].

Fig. 10. Increasing the density of 'leaky' transistors was projected

transistors with a feature size of 10 micrometers as shown in figure 4. Intel's newest microprocessor, scheduled to be released late in 2007, has 410 million transistors with a nominal feature size of 45 nanometers, as shown in figure 5. According to figure 3, the 45 nanometer devices should have a gate length of only 25 nanometers.

4. Advanced Transistors

Long-range planning for development and production of ever-smaller transistors requires a 'roadmap' of dimensions and technologies. Figure 6 shows a recent transistor roadmap for the first two decades of the 21st century. Devices with 90 nanometer transistors are being phased out while devices with 45 nanometer transistors are being readied for production. One feature common to most of these advanced transistors is carrier mobility enhancement through carefully engineered strain in the channels. PMOS transistors are in compression through epitaxial silicon germanium grown source-drain regions as shown in figure 7, whereas

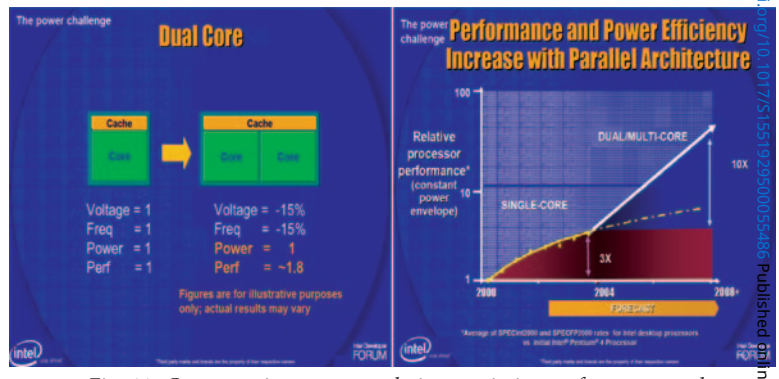

Fig. 11. Current microprocessor designs optimize performance and efficiency by reducing how hard the transistors are driven and re-gain performance by utilizing multiple cores[2].

Fig. 12. Multiple-core microprocessors are the key to continuing performance improvements in the future[2].

NMOS transistors are put in tension by nitride films applied to the outside of the transistors as shown in figure 8. Beyond simple shrinkage, new designs such as trigate, carbon nano-tube, silicon or germanium nanowire, and III-V superlattice designs are on the development roadmap.

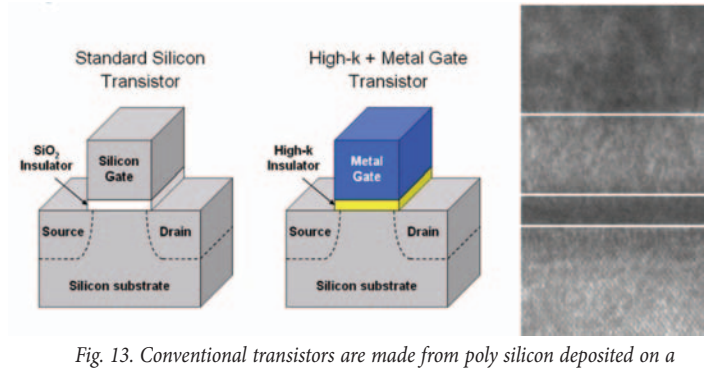

Fig. 13. Conventional transistors are made from poly silicon deposited on a silicon-oxide insulator[2].

Fig. 14. The new high-k metal gate transistors use a metal layer on a hafnium- based insulator[2].

Fig. 15. TEM micrograph of the new high-k metal gate[2].

Another feature of high performance transistors that needed to be addressed was their high power consumption. Current flow through the transistor when the transistor is supposed to be off, combined with current leakage through the gate, wastes energy and

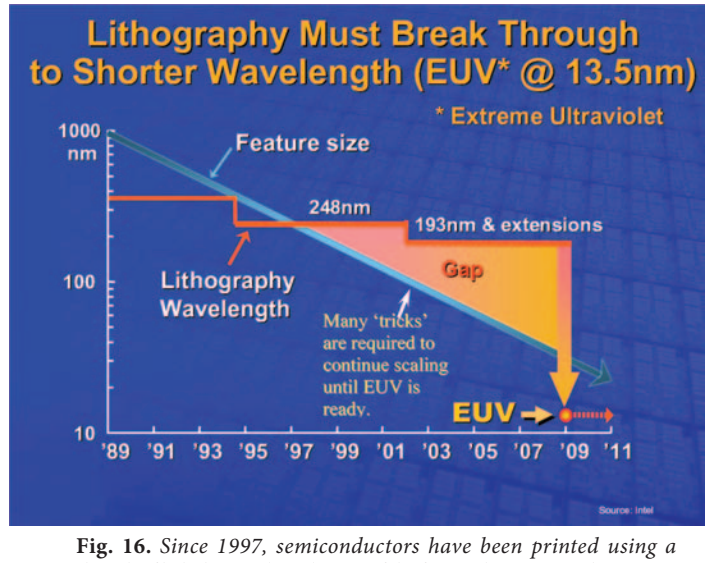

Fig. 16. *Since 1997, semiconductors have been printed using a wavelength of light longer than the size of the feature being printed. Extreme Ultra Violet lithography will not be ready until 2009[2].*

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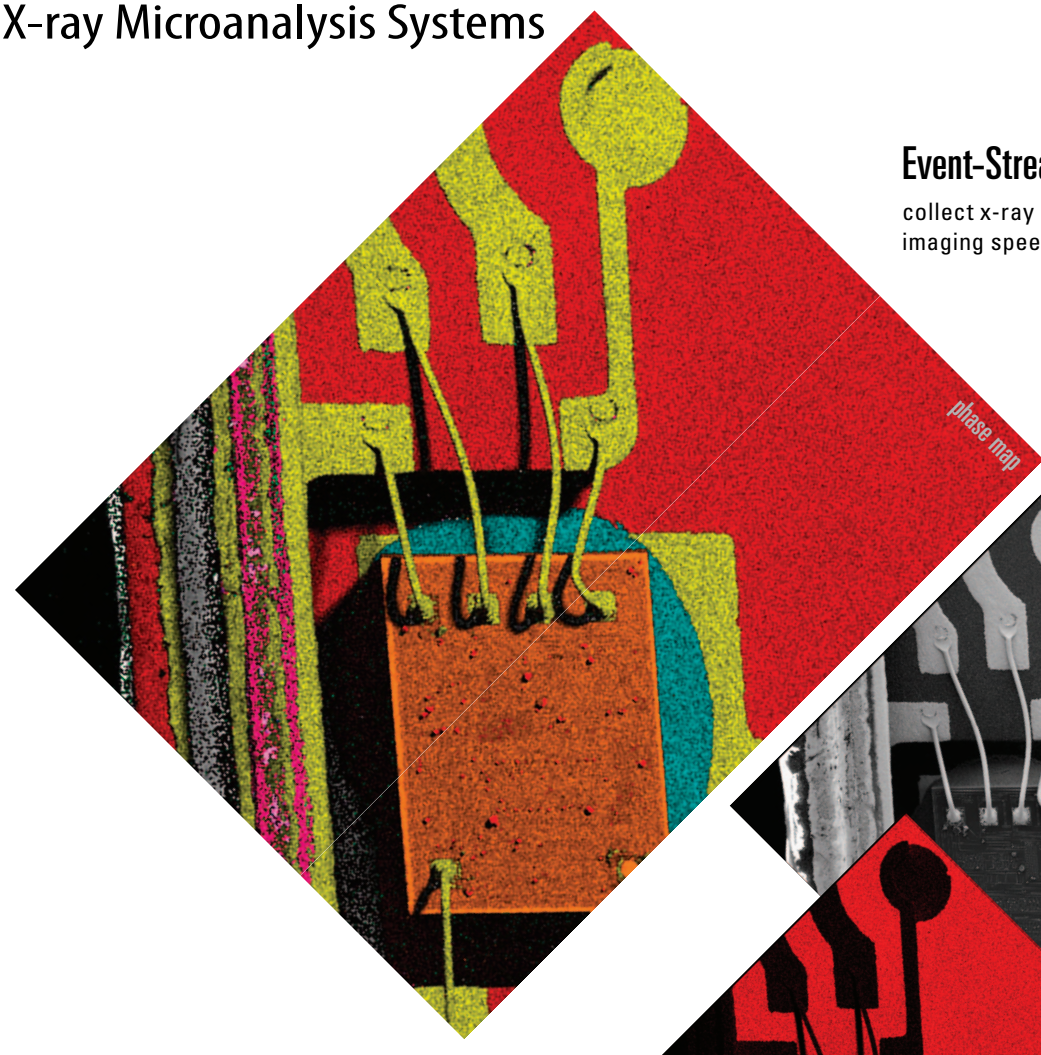

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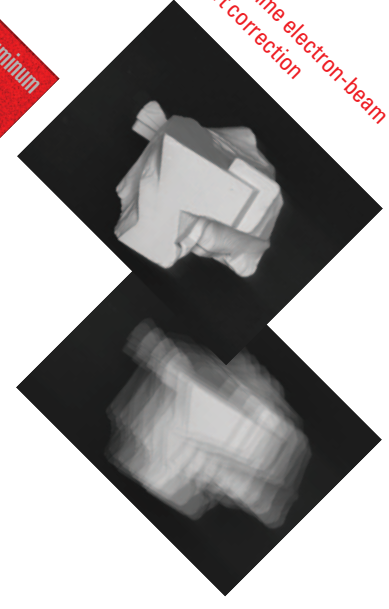

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Fig. 17. Extreme Ultra Violet lithography will not use conventional projection optics, but will rely on reflection from patterns on dielectric mirrors[2].

Fig. 18. EUV machines are huge and expensive, as can be seen in this photograph of a prototype tool at SUNY Albany[3].

produces excessive heat. Figure 9 shows where the excess current flows in a transistor when it should actually be turned off: through both the gate and the channel. High leakage per transistor combined with growing transistor density could result in thermal loads that could not be dissipated, resulting in extreme temperatures that would melt any device, as shown in figure 10. Today's solution to this dilemma is to reduce the performance of individual transistors just slightly, with tremendous benefits in efficiency, and then increase the number of 'cores' to re-gain performance. Figure 11 shows how the 'dual core' strategy enhances performance and efficiency. Dropping the voltage and speed by 15% can cut the power consumption in half while dropping performance by only 10%. Adding a second core increases power consumption back to where it was before, but then the total performance of the two cores working together can be 80% greater than that of the single core working alone. Projections are that multiple core microprocessors will be the trend of the future as microprocessor efficiency becomes equal in importance to raw performance.

Another key development is a change in gate dielectrics. Thinner gate dielectrics allowed the field in the channel to be strong enough to switch the transistors on or off with lower applied gate voltage, but gate dielectrics could not be made to function reliably when they were thinner than two silicon unit cells. Changing to a hafnium-based high-k dielectric allowed a much thicker dielectric. Eliminating the silicon above the dielectric removed a charge depletion region that unpredictably influenced the switching voltage of the transistor. Figures 13 and 14 show schematics of these two transistor strategies, and figure 15 shows a TEM micrograph of part of the new gate.

5. Lithography Challenge

Since 1997 microprocessors have been made by printing features using optical lithography with a wavelength (193nm) longer than the size of the features being printed. Until optical lithography is replaced by Extreme Ultra Violet (EUV-13.5nm), a number of tricks will be required to continue producing devices with progressively smaller dimensions. Optical proximity correction is a technique altering the projection pattern so that interference within the transmitted plane wave will produce the desired pattern on the wafer. Multiple patterning strategies use multiple exposures to refine the pattern being produced on the wafer. Finally, immersion lithography, in which the final lens and wafer are immersed in a fluid, increases the effective numerical aperture of the optics to improve the effective resolution and depth of focus.

Extreme Ultraviolet Lithography (EUV) promises to solve the dilemma of printing features smaller than the wavelength of light. At 13.5 nanometers wavelength, EUV is the wavelength of choice for the future. Since this wavelength cannot pass through any known lenses, the optics rely on dielectric mirrors to focus the light, and the patterns need to be deposited on dielectric mirrors, as shown in figure 17. Since EUV also cannot pass through air, the entire tool needs to be inside ultra high vacuum. From the 13.5 nm source to the UHV chamber and optics, these machines are huge and expensive, as can be seen in the photograph in figure 18.

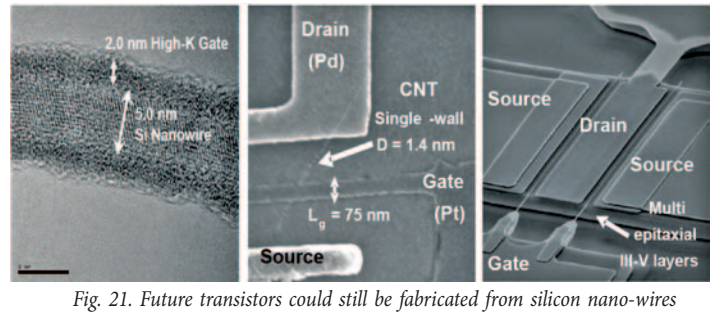

Fig. 21. Future transistors could still be fabricated from silicon nano-wires surrounded by the gate[2].

Fig. 22. Carbon nanotubes are another candidate for future transistors[2].

Fig. 23. III-V quantum-well transistors are also contenders, but will need integration of high-k dielectric gates[2].

6. Future Transistors

One attractive strategy for advanced transistors would have the channel surrounded on all sides by the gate, as shown in figure 19. This transistor geometry could have the highest efficiency and speed, but would provide great challenges for mass production. An alternative that could also have excellent efficiency and performance, yet still be suitable for volume production, is called a 'tri-gate' transistor, as shown in figure 20. Three other transistor designs that are still being researched are silicon nanowires, carbon nanotubes and III-V quantum well superlattice devices as shown in figures 21, 22 and 23. However these approaches are all in the research stage, and volume manufacturing could be a decade away.

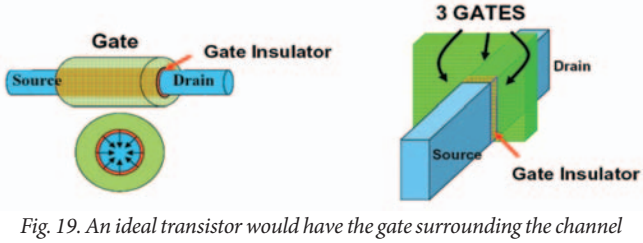

Fig. 19. An ideal transistor would have the gate surrounding the channel and would have the highest power efficiency possible[2].

Fig. 20. The Tri-Gate transistor approaches this power efficiency and promises better manufacturability[2].

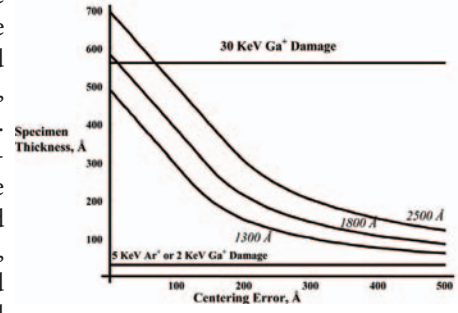

Fig. 24. Specimen preparation requirements for obtaining clear interpretable images of features comparable to that of traditional TEM specimens are challenging. The specimen thickness and centering of the cross-section onto the center of the feature must fall below curves in this plot, and the amount of damage on the surface caused by the ion beam must be a small fraction of the total specimen thickness[4].

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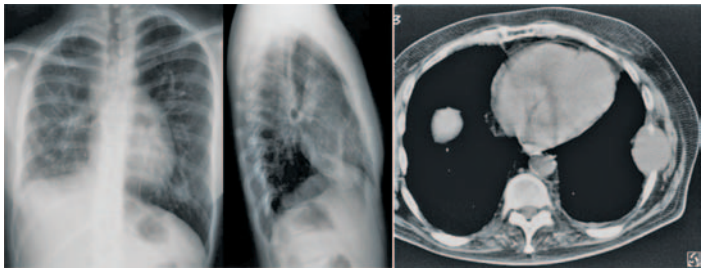

Fig. 25. Medical radiographs are analogous to TEM specimens in which the specimen thickness is comparable to the size of the objects being examined.

Fig. 26. Computed Axial Tomography holds the promise of creating virtual cross-sections of objects that challenge the ability of our 'real' cross-sectioning capability.

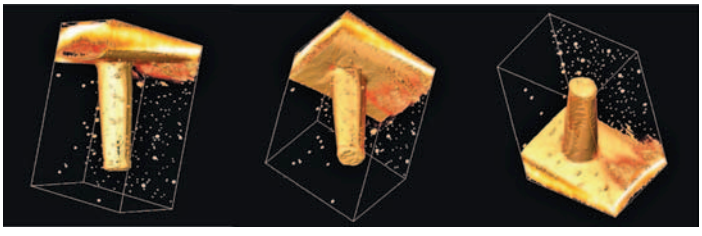

Fig. 27. Three different views of a vertical metal interconnect reconstructed from a tilt series using high angle annular darkfield Scanning Transmission Electron Microscopy (STEM)[5].

7. Microscopy Challenges

The Transmission Electron Microscope (TEM) has been one of the most important tools for characterizing the morphology and dimensions of semiconductor features for many years, and will be even more important in the future. However, changes in the structure of semiconductor devices will require changes in our methods and approach. Three-dimensional transistors with dimensions significantly smaller than the mean free path of 200KV electrons will require very special cross-sectioning techniques. Dual beam Focused Ion Beam (FIB) tools with which one can view a specimen with improved contrast and resolution for centering the specimens will be essential. Specimens will need to be made 10-20 nm thick on a regular basis. Figure 24 illustrates some of the challenges. When the specimen is not centered within a nanometer, it needs to be dramatically thinner to preserve the fidelity of the image. Furthermore, at these dimensions, any surface amorphous layers are not tolerable. The specimen surfaces must have an abrupt transition from bulk to vacuum. Eventually, tomographic techniques will be needed to supplement cross-sectioning. Figures 25 and 26 show how x-ray tomography can provide virtual cross-sections of specimens that cannot be cross-sectioned, and figure 27 shows how tomography has been used to image vertical interconnects. However, improvements are needed in automation, resolution, and contrast before tomography can fulfill its promise in the semiconductor industry. ■

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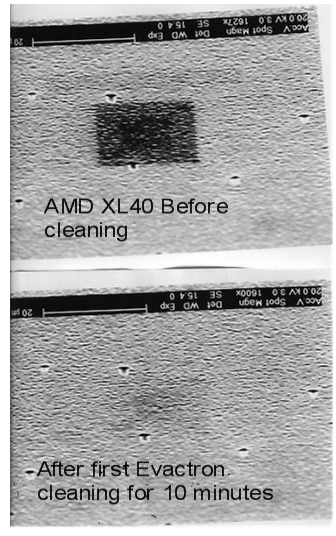

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