NATO Advanced Study Institute Explores Microelectronic Materials

"Microelectronic Materials and Processes" is the topic of a NATO Advanced Study Institute (ASI) which will be held from June 30 to July 11, 1986 in Castelvecchio Pascoli, Italy. NATO ASIs are primarily high-level teaching activities at which carefully defined subjects are presented at a post-doctoral level.

The objectives of this ASI are to (1) provide an international forum for presentation and discussion of key topics in the science and technology associated with the development of very large-scale integrated (VLSI) silicon circuits; (2) identify specific research areas where new contributions in the fields of materials science and process engineering can yield significant improvements in IC device performance; (3) outline the fundamental limitations of current microelectronic fabrication technologies and address future materials and processing needs; and (4) help integrate complementary inter- and intra-national research efforts into viable and competitive production techologies. In the program that follows, 15 key topics, covering all major materials and processing steps used in the fabrication of VLSI silicon circuits, will be presented by eminent lecturers drawn from academia and industry.

W. Fichtner, Swiss Federal Institute of

Technology (ETH), Zurich, Switzerland: "Process Simulation"

H. W. Werner, Phillips Research Laboratories, Eindhoven, Netherlands: "Diagnostic Techniques for Microelectronic Materials"

This ASI will be held at the "Il Ciocco" Hotel and Conference Center, Castelvecchio Pascoli, Italy, which is located approximately 60 km north of Pisa in the province of Lucca. The total cost of participation, per person, per day, including accommodations, three meals, coffee breaks, and conference facilities will be approximately U.S. \$400.00 (double) and U.S. \$500.00 (single). The conference fee of U.S. \$400.00 also includes a copy of the proceedings. Limited financial support is available for those who apply for assistance.

ASIs are small-size meetings with lectures on research findings and applications given by a selected team of international experts. These speakers are also at the disposal of the participants throughout the meeting for informal personal and roundtable discussions. Specific subjects can be dealt with at the right depth and level of confidentiality, in a relaxed atmosphere conducive to free-ranging discussions.

Total attendance will be limited to 100 participants. Deadline for applications will be May 5, 1986. For further information, contact R. A. Levy, NATO ASI Director, AT&T Bell Laboratories, Murray Hill, New Jersey 07974; (201) 582-7375, Telex: 219348

or 138650.

E. Bauser, Max Planck Institute, Stuttgart, West Germany: "Crystal Growth and Epitaxy"

G. J. Declerck, Catholic University of Leuven, Leuven, Belgium: "Silicon Oxidation"

W. Westwood, Bell Northern, Ottawa Canada: "Physical Vapor Deposition"

W. Kern, RCA Laboratories, Princeton, New Jersey: "Chemical Vapor Deposition" and "Dielectrics"

S. P. Murarka, Rensselaer Polytechnic Institute, Troy, New York: "Silicides for VLSI Applications"

C. Grant Willson, IBM Research Laboratory, San Jose, California: "Resist Materials"

A. N. Broers, University of Cambridge, Cambridge, England: "Fine-Line Lithography"

D. W. Hess, University of California, Berkeley, California: "Dry Etching Processes"

E. Rimini, University of Catania, Catania, Italy: "Ion Implantation"

U. Gosele, Duke University, Durham, North Carolina: "Diffusion in Semiconductors"

Y. Pauleau, CNET, Grenoble, France: "Interconnect Materials"

K. V. Ravi, Mobil Research Center, Waltham, Massachusetts: "Imperfections and Impurities in Semi-conductors"

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