# Correlative Defect Characterization in Semiconductors via Electron Channeling Contrast Imaging and Scanning Deep Level Transient Spectroscopy

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Sub-bandgap electronic defect levels in semiconductor materials often produce deleterious effects within associated devices, from generally poor performance to unpredictable reliability to outright degradation. Because these electronic states are effectively always the result of some kind of structural defect—impurities, vacancies, dislocations, grain boundaries, etc.—if one can identify the physical source, then one can ostensibly develop strategies for the elimination, or at least mitigation, of the offending defect. Nonetheless, precisely identifying those sources is, more often than not, exceptionally difficult and time-consuming. For example, in the case of epitaxial semiconductors, it is well-known that threading dislocations tend to be introduce charge carrier traps, but exactly which trap levels belong to which defects, and thus the fundamental nature of the resultant electronic states, is generally not well understood.

To this end, we discuss here work combining SEM-based electron channeling contrast imaging (ECCI) [1,2] with a novel scanning Kelvin probe based deep level transient spectroscopy technique (scanning-DLTS) [3,4] toward the identification of the microstructural source of a specific defect level with an ideal model system: the infamous $E_C - 0.57$ eV electron trap in $n$-type GaN. ECCI has previously proven to be a convenient and effective technique for non-destructive structural characterization across a range of materials, including in correlation with cathodoluminescence imaging [5]. Scanning-DLTS has, more recently, been shown to provide valuable insight into the distributions of deep level traps in various semiconductors. But it is the direct correlation of the two creates a truly unique and powerful capability for semiconductor defect characterization.

The $n$-type GaN sample investigated in this study was grown by $NH_3$-based molecular beam epitaxy with an $n$-on-$n^+$ structure, produced on a sapphire substrate. The top-most $n$-GaN layer was Si-doped to nominally $3 \times 10^{16}$ cm$^{-3}$. Schottky diodes—needed to enable band modulation for the filling and emptying of traps—were formed via standard lithographic methods. Thin (8 nm) Ni pads on the top $n$-GaN yielded Schottky contacts while Ti/Al/Ni/Au pads on the underlying $n^+$-GaN provided Ohmic contact. Scanning-DLTS was performed using a customized scanning Kelvin probe system, described in detail elsewhere [3,4]. ECCI was performed in an FEI Sirion field-emission SEM, operated at 25 kV accelerating voltage and using a pole-piece mounted annular backscattered electron detector.

Elucidation of the $E_C - 0.57$ eV trap level, which is a major source of reliability problems in GaN-based high electron mobility transistors (HEMTs), has eluded researchers for over two decades [6,7]. However, by linking the surface spatial- and energy-resolved trap distribution mapping of scanning-DLTS (see Figure 1) with the dislocation-resolved diffraction contrast imaging/characterization of ECCI (see Figure 2), we have discovered a direct, site-to-site correlation between the $E_C - 0.57$ eV trap level and pure edge dislocations in GaN (see Figure 3). Screw and mixed dislocations, on the other hand, show a complete lack of correlation with this state. Although this identification does not yet ascribe exact causality, it has

provided more direct evidence as to the source of this state than two decades worth of prior indirect investigation. Furthermore, this work provides an excellent example of ECCI's position as an ideal correlative imaging partner with any number of different surface and scanned-probe methods, including for the analysis of fully processed electronic devices [8].

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**Figure 1.** (*top*) AFM topography image and (*bottom*) scanning-DLTS concentration map of the $E_C - 0.57$ eV trap distribution across the region of interest. The scanning-DLTS map is taken from the region indicated by the dashed white lines.



**Figure 2.** (*left*) Electron channeling pattern on the patterned sample for diffraction orientation. (*top*) ECCI micrograph taken in a $\mathbf{g} = [\bar{1}2\bar{1}0]$ diffraction conditions of the same sample region in Figure 1.
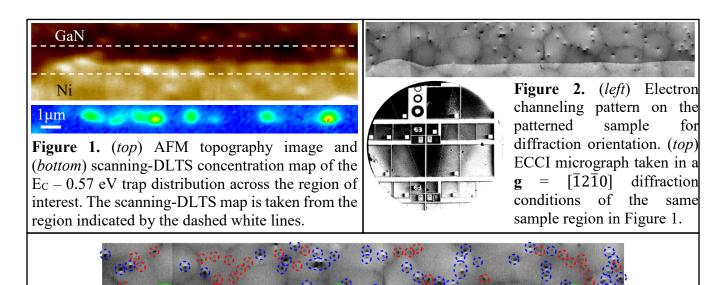


**Figure 3.** Correlative overlay of the scanning-DLTS concentration map (from Fig. 1) on the ECCI micrograph (from Fig. 2). Standard $\mathbf{g} \cdot \mathbf{b}$ analysis over multiple $\mathbf{g}$ conditions was used to determine dislocation type, indicated by either red (pure edge) or blue (screw or mixed) circles. The thick, black dashed line indicates the calculated depletion edge for the trap emptying diode bias conditions, beyond which the scanning-DLTS sensitivity begins to fall off, yielding an ~1 μm sensitivity distance from the Ni metal edge. Dislocations with solid circles are outside the nominal depletion region, and thus will experienced reduced sensitivity for scanning-DLTS detection, while dashed circles indicate are within the expect. Note that some dislocations are visible beneath the Ni contact pad, but with insufficient contrast to enable geometry identification.