Application of Advanced Back-Side Optical Techniques in ASICs

Douglas Martin,[1] * Samuel Beilin,[2] Brett Hamilton,[1] Darin York,[1] Philip Baker,[1] and Wai-Yat Leung[1]

[1]Naval Surface Warfare Center, 300 Highway 361, Crane, IN 47522

[2]Charles Stark Draper Laboratory, 555 Technology Square, Cambridge, MA 02139

*douglas.martin@navy.mil

Introduction

Failure analysis is important in determining root cause for appropriate corrective action. In order to perform failure analysis of microelectronic application-specific integrated circuits (ASICs) delidding the device is often required. However, determining root cause from the front side is not always possible due to shadowing effects caused by the ASIC metal interconnects. Therefore, back-side polishing is used to reveal an unobstructed view of the ASIC silicon transistors. This paper details how back-side polishing in conjunction with laser-scanned imaging (LSI), laser voltage imaging (LVI), laser voltage probing (LVP), photon emission microscopy (PEM), and laser-assisted device alterations (LADA) were used to uncover the root cause of failure of two ASICs.

General Discussion of Optical Techniques Used in Failure Analysis

LVI and LVP [1] are fairly recent optical beam techniques that rely on monitoring the expansion and contraction of the transistor space charge region (SCR), caused by the device being electrically exercised. Their utility is most effective when laser transmission/reflection occurs through linear homogenous materials such as silicon or silicon dioxide substrates, as commonly observed on the back side of wire-bonded integrated circuits (ICs). An optimum laser wavelength for use with silicon optical properties is 1340 nm. The incident laser light on the back side of the integrated circuit is modulated in accordance with the oscillation of the SCR. Figure 1 shows an n-channel metal oxide semiconductor field effect transistor (MOSFET), where the absence (off) and presence (on) of the SCR are illustrated in A and B, respectively; the SCR is highlighted in B with the "1" and "2" arrow indicators.

Figure 2 shows a LVI test setup on the left and a LVP test setup on the right. In both cases, an avalanche photodiode is used as the detector. LVI relies on the frequency of the transistor oscillation, which is controlled by the digital tester when the device under test (DUT) is exercised. Providing the controlling frequency at which transistors are being turned on and off to a spectrum analyzer enables an image overlay for the laser-scanned image. The overlay shows which transistor space charge regions are operating at the given frequency. Comparing the image and overlay of a good device to a suspect device allows suspect regions to be located.

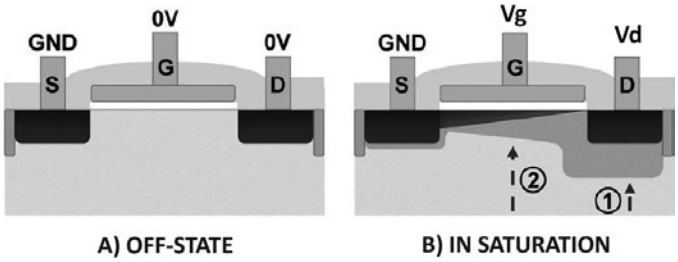

Figure 1: Contraction and Expansion of the SCR of a MOSFET [2]; reprinted with permission from Elsevier.

LVI uses a scan generator for XY imaging and a spectrum analyzer to detect regions of a given SCR oscillation, whereas LVP uses the LVI overlay to determine where to locate the laser in spot mode over an SCR. An oscilloscope acquires the timing waveform when the transistor switches on and off. Inputs to the DUT and a trigger for the oscilloscope are provided by the digital tester. By comparing the timing waveform of a good device to a suspect device, one can observe whether a circuit node on an IC is functioning or not.

Although LADA [3] can be used as a back-side technique, it is more effective on the front side if the failure is associated with metal interconnects. Unlike LVI and LVP, which are used to monitor transistor behavior, the laser in LADA is used to *alter*

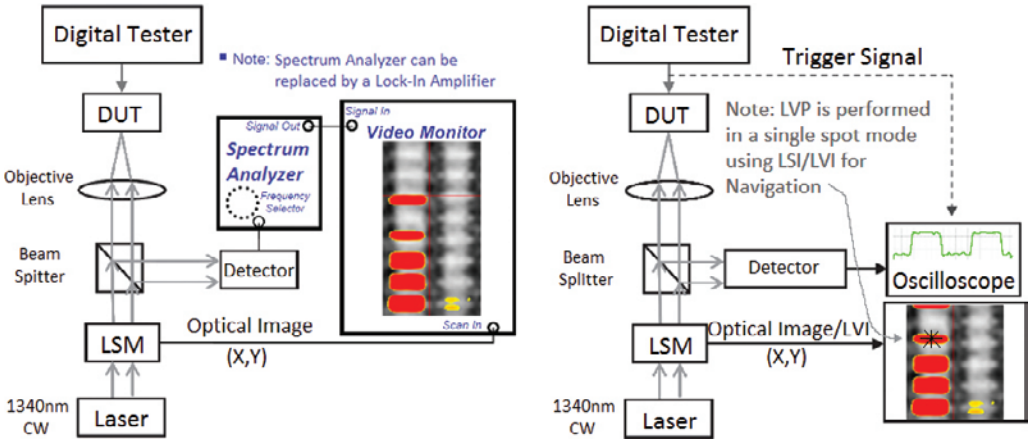

Figure 2: LVI and LVP test setups, left and right, respectively. On the left, the beam is scanned over a region of interest to produce the LVI image, whereas on the right the beam is fixed at * to track the variations in the SCR [2]; reprinted with permission from Elsevier.

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the transistor behavior. For this application of LADA, it is a technique *assisted* by digital tester pass/fail feedback to isolate where laser stimulation causes failure, provided the laser stimulation has the fidelity of the failing environment. Fidelity is assured by demonstrating that stimulated equivalent transistor structures function (pass), while the suspect region fails. LADA's niche is that it is particularly effective for intermittent failures. Because intermittent failures can be forced into a failing mode during laser irradiation, circuit defect localization can be accomplished. LADA is a method that requires two trigger signals. One trigger signal tells the machine when the laser can step to the next pixel in the image, after performance of a digital test. The other trigger signal is a conditional pass/fail test, in which a flag is raised when a fail result is processed by the digital tester. This signals the instrument to show failure locations in the form of an image overlay within a particular region of the LSI image, representing a portion of the circuit.

Two other useful techniques are LSI and PEM, which can be used on either the front side or back side of the device. LSI requires no electrical stimulation of the device; it is simply an optical image of the device, generated using a laser. Because the transistor feature size can be similar in magnitude to the wavelength of the laser, different laser wavelengths enhance different sets of features, associated with different transistor fabrication process steps. In addition to the 1340 nm laser, the 1064 nm wavelength is also commonly used.

PEM [4] requires electrical inputs and is usually the optical technique of choice. Any transistor or diode action will result in current leakage and generate electron hole pairs, which will produce photon emission in the infrared region. Through integration over a given exposure time, an image overlay can be generated to compare a good device to a failing device to determine whether a region is suspect.

First Investigation: Failure Within the Sea of Gates

The electrical fault signature of the first investigation was that the ASIC functioned correctly passed at low-clock frequencies but failed at clock frequencies above 2 MHz. Acceptance testing was clocked at 500 KHz, and therefore this failure was not detected until it was installed onto a module. Using PEM from the front side of the device, a region of the device clearly showed photon emission different from the control device when exercising it at a clock frequency of 20 MHz, as shown by the photon emissions enclosed in rectangles in Figure 3. The brightest emission of the failing device was not observed in the control device.

From the schematic and layout information, it was determined that the rectangles enclose a D-type master/slave flip-flop circuit. When performing PEM on the brightest emission at various clock frequencies, a threshold frequency was clearly demonstrated (Figure 4).

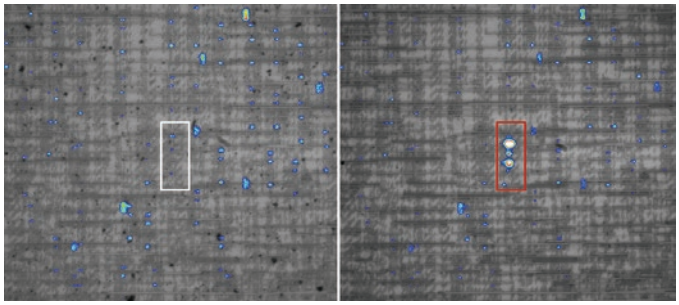

Figure 3: PEM from the front side of a control device (left) and a failing device (right) when clocked at 20 MHz.

After using back-side polishing tools to drill through the package, the die was then polished to prepare a silicon window for LSI. A laser-scanned image was taken at wavelengths of 1340 nm and 1064 nm, as shown in Figure 5. Although the 1064 nm image on the right clearly shows more transistor detail, the interruption of the white columns is more revealing of root cause and is abnormal for this sea of gates portion of the ASIC.

The flip-flop circuit that was observed on the front side using PEM overlapped the abnormal region on the back side. Because LVI was being performed, it was important to understand that the flip-flop circuit, in conjunction with the way that it was exercised by the digital tester, has a clock frequency that is 4× that of the input (or output) on/off frequency. To determine if the abnormal region was indeed a processing issue, LVI was used to check the functionality of the circuit at two different clock frequencies (500 kHz and 20 MHz). The frequency settings for LVI were 125 kHz/500 kHz and 5 MHz/20 MHz. The LVI images of the most active column of the flip-flop circuit were monitored, and a comparison between the failure and the control was performed (as shown in Figure 6). The LVI locations as shown by the transistor positions for the 125 KHz/500 KHz comparison are nearly identical except for the abnormal region. The 5 MHz/20 MHz LVI in Figure 6 show differences at other transistor positions outside the abnormal region, due to those transistors being downstream from the affected region.

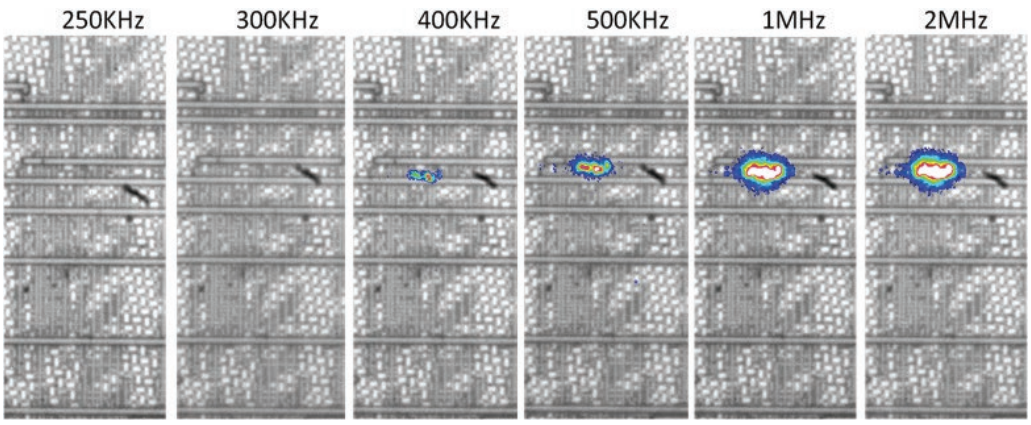

Figure 4: Brightest photon emission of the failing device at various clock frequencies.

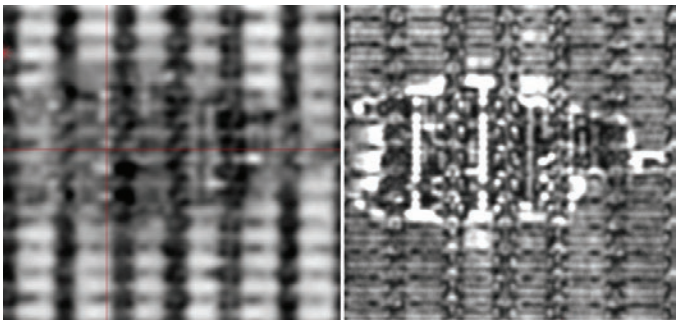

Figure 5: LSI of failure location from the back side in the first IC investigation. Two laser wavelengths were used: 1340 nm (left) and 1064 nm (right).

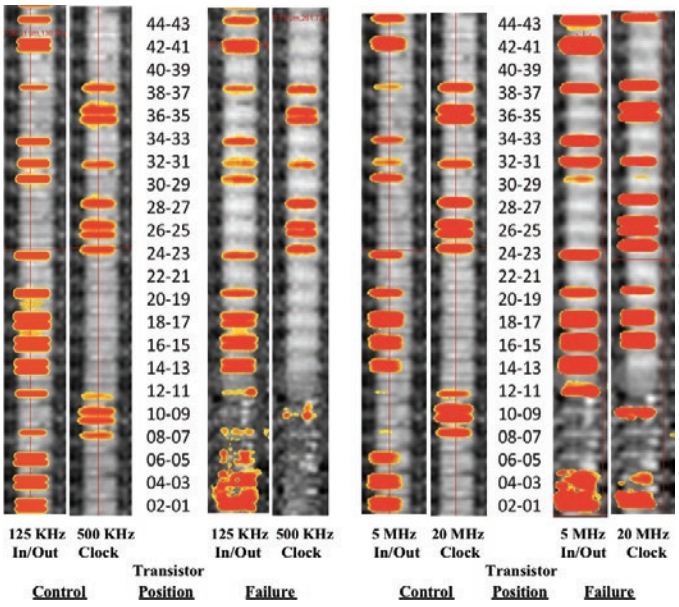

Figure 6: LVI control/failure comparison at 125 KHz/500 KHz and 5 MHz/20 MHz (in–out/clock; frequency).

In hindsight, this example investigation illustrates that LVI is best used near the frequency threshold (as supported by data in Figure 4) when the device is passing, for frequency-related failures of this type. It also demonstrates that if an intermittent cannot be easily made to fail as interpreted by a digital tester, the deleterious effects can still be observed using LVI (PEM also).

The spot mode measurements performed when taking LVP timing waveforms are shown in Figure 7 for the 20 MHz clock rate. The timing waveforms observed at positions 10, 9, 4, 3, 2, and 1 fall within the abnormal region observed in the LSI, and the control is expected to be different from the failure, because the device is in a failing mode (as interpreted by the digital tester). At transistor position 20, LVP (timing waveform) is consistent with the LVI at this position in the failing device, which differs from the LVI and LVP of the control device at this position, even though it is outside the abnormal region. This is because the circuitry at position 20 is downstream from the circuitry within the abnormal region. When the device is passing near the threshold frequency (500 KHz clock rate) that failures occur, the LVI and LVP (timing waveforms for this clock rate are not in this

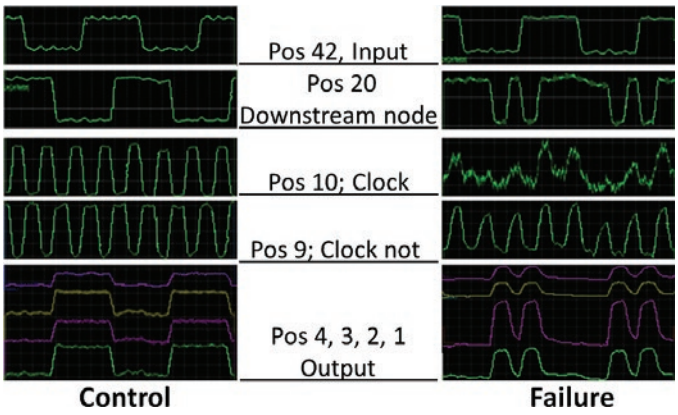

Figure 7: LVP timing waveforms; control versus failing device; the position ("Pos") numbers in the center can be traced back to the positions in the LVI of Figure 6; conclusive evidence that transistors within the abnormal region have the same frequency-related characteristics of the failure.

paper) data are identical except for the abnormal region of interest where the damage is located.

Of course once a failure is deprocessed using the Focused Ion Beam/Scanning Electron Microscope (FIB/SEM), no further electrical investigation is able to be performed. Therefore, the investigation process must be thoroughly vetted. To summarize the investigation, the LSI shows that the abnormal region overlaps the failing flip-flop. LVI and LVP demonstrate that the transistor frequency behavior characteristics within the abnormal region are consistent with the original failure characteristics on the module.

Figure 8 shows FIB/SEM deprocessing inside and outside the abnormal region observed in Figure 5. Six contacts connecting six transistors with metal 1 are shown in Figure 8. The left side is normal and the right side is not; the abnormal transistors are encircled by the red oval in Figure 8. The four transistors within the red oval have missing titanium silicide. It can now be explained that the interruption of the white columns in the 1340 nm LSI image of Figure 5 is due to missing titanium silicide. Titanium silicide is conductive and provides a low-resistance (ohmic) contact. When titanium silicide is missing, a Schottky junction is formed, which has parasitic impedance at high frequency.

The abnormal region was formed when a foreign particle was introduced just prior and/or during the silicidation step of the die fabrication. The particle was then removed during a subsequent cleaning process step.

Second Investigation: Failure Within the Embedded Memory of an ASIC

The second investigation was a single bitcell failure in the embedded memory of an ASIC. The intermittent failure was not observed at ambient temperatures during acceptance testing. However, after exposure in a Cobalt 60 irradiator, the same electrical screen test demonstrated that there was a single bitcell failure, which was uniquely identified. After baking the device for 168 hours at 125 degrees Celsius, the device started passing again.

Figure 9 shows at least 12 embedded memory bitcells in each of the two laser-scanned images, which also include the

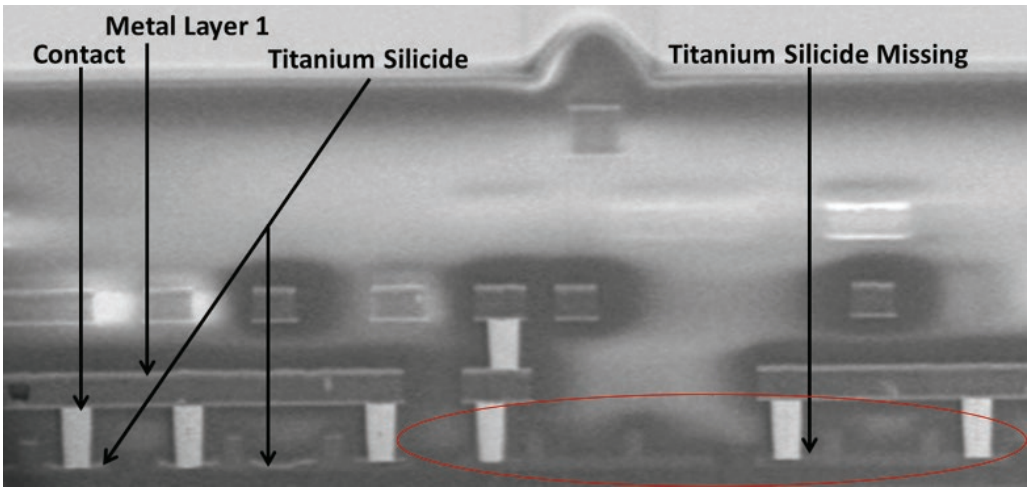

Figure 8: Deprocessing via FIB/SEM; the transistors within the red area show they are missing titanium silicide on the right; the transistors on the left side of the image are normal.

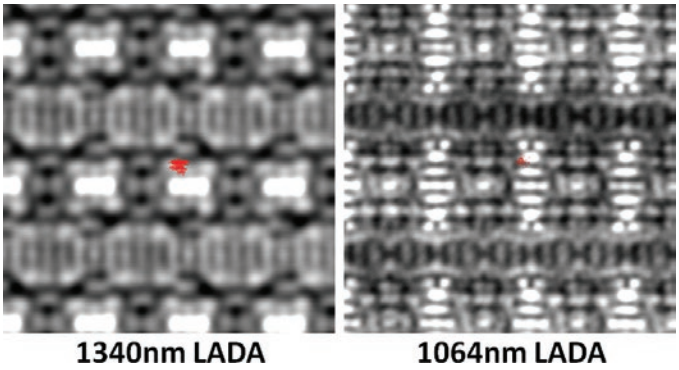

Figure 9: LADA shows the region that caused failure (red pixels) in the second IC investigation: 1340 nm laser (left) and 1064 nm laser (right).

failing bitcell in the center of the image. LADA demonstrated that both the 1340 nm and 1064 nm laser wavelengths could generate enough local heat to cause the failure to reoccur. LADA was *assisted* by digital tester feedback to give pass/fail status for every pixel in the laser-scanned image; a red pixel overlay in Figure 9 shows when failures were indicated. Because the surrounding bitcells had a passing status consistent with the original fault signature, it was deemed that laser *alteration* demonstrated the fidelity required to replicate the failure in this fashion. LADA provided accurate localization of the failing transistor. Both images of Figure 9 have equivalent magnification and position.

The LADA failure localization provided an accurate means of navigation for FIB deprocessing. The FIB/SEM deprocessing shown in Figure 10 illustrates two different FIB cross sections in the failing transistor. The sidewall spacer oxide on both sides of the polysilicon should be symmetric. In this case the sidewall spacer on the left of the polysilicon is collapsed, which led to an absence of protection afforded to the critical gate oxide/channel region during the titanium silicide process step. Voids are observed in the image to the left in Figure 10, which indicates the absence of a foreign particle that was once present during critical fabrication process steps. The foreign particle was later removed during subsequent processing steps. Upon further cross sectioning of this region, a titanium silicide gate to source bridging fault is observed.

Conclusion

The frequency-dependent intermittency in the first investigation highlighted that LVI and LVP could be effectively applied to observe defective transistors when the failure was in a passing condition.

In the second investigation the defect was not revealed in the LSI, and FIB/SEM determined the failure site to be much smaller than the two wavelengths used in the LSI. Laser stimulation was required for the temperature-dependent intermittency of the second investigation, in which the stimulation was provided by LADA to isolate the failure location.

The application of advanced back-side optical techniques was used in the failure investigation for two ASICs. Both

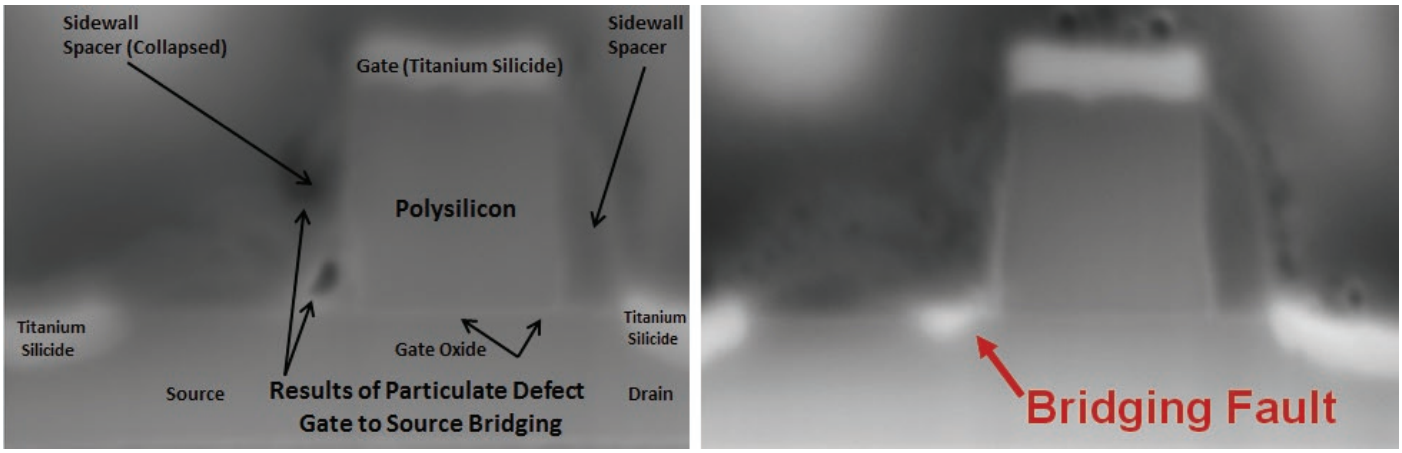

Figure 10: The FIB deprocessing shows a bridging fault in the second investigation. This bridging fault resulted in a gate to source short.

investigations determined that the introduction of a foreign particle at a particular step in the fabrication process was the root cause of the failures. Appropriate corrective actions resulted from the failure analysis investigations.

Acknowledgments

As a master in the skill of active listening, Fred Barsun has effectively multiplied his analytical methods, which include the subject matter in this work. The assistance and advice of Matt Sale tailored our investigative approach and achieved the design needs for these analyses. Relying on Jack Henderson's equipment and materials expertise helped in transforming the back-side polishing methods from a pioneering stage to maturity.

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