

Image Simulation and Analysis to Predict the Sensitivity Performance of a Multi-Electron Beam Wafer Defect Inspection Tool

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Electron beam inspection systems are sensitive to sub-10 nm critical defects however the throughput of single electron beam tools is orders of magnitude below high volume manufacturing (HVM) requirements. Using multiple electron beams within a single tool is an approach that can overcome the above deficiency. As such, SEMATECH initiated a program to hasten the development and commercialization of massively parallel multi-electron beam inspection technologies [1] [2]. Key to the program was to cultivate the design and specification conditions for an HVM tool. Program details and objectives of facilitation have been presented hitherto as well as a discussion of relevant hardware [2] [3]. Crucial to framing system needs is to comprehend in what way various changes to device design or working conditions effect throughput and defect sensitivity for a given use case. To enable this objective, a set of simulation programs was designed to model tool performance and forecast system sensitivity to various types of defects. Rigorous simulation tools enable several objectives: (1) allow large parameter space to be assessed economically, (2) optimize tool design by rapid exploration of operating condition parameter space, and (3) predict performance of the system for new device architectures and application spaces. Generation and analysis of realistic virtual samples with archetypal defects requires a number of steps. Briefly, steps include (1) creating a pixelated virtual sample containing defects, (2) simulating nominal electron emission behavior, (3) simulating an image by modulating the emission behaviors with dose-dependent shot noise and instrumental artifacts, and (4) analyzing the resultant image to assess the noise tolerance of the defect signature signal strength as a function of defect size. This process is illustrated graphically in Figure 1. A more detailed version has been provided elsewhere [4].

In HVM, defects such as broken lines, bridged connections, and particles occur at a low concentration (e.g., < 10 per 300 mm wafer). To simulate full wafers with scant defects at nanometer resolution would be prohibitive in computational time. To generate images in sizes akin to those expected from the tool, in practical amounts of time, a unit cell of a repeating structure is simulated so as to include an exact match of the pixel size to the pitch of the structure, allowing smaller images to be tiled in a modular scheme. Defect blocks are created by altering an ideal block by adding a set type and size of defect. Tiling ideal and defect blocks are used to create a large scale virtual sample. The simulated defect pattern types and sizes mirror the physical Intentional Defect Array (IDA) test wafers that are produced by SEMATECH for assessing metrology tool performance.

Tiled images are subsequently analyzed using an algorithmic process developed in conjunction with NIST. In this process, sensitivity analysis of defects provides a quantitative means of analyzing the relative strength of the defect signature in a real or virtual image. A differential image is obtained by subtracting two ostensibly identical images; a defect free reference image and a test image containing a defect. In this program, the defect signature is the signal-to-noise ratio (SNR) of the differential image, i.e. the remaining image of the defect comparative to the noise difference. This SNR calculation, although not an actual defect inspection algorithm, may be used as a benchmark to weigh the effect of

defect size, material contrast, image dose, tool performance, detector noise, etc. The trends projected by this analysis imitate the impact of tool design, sample variations, or operating conditions on the ability of an actual inspection algorithm to detect defects. Figure 2 illustrates this process [5].

References:

[1] Thiel, B. *et al.*, “Assessing the Viability of Multi-Electron Beam Wafer Inspection for sub-20 nm Defects”, Proc. SPIE 9236, Scanning Microscopies 2014, 92360E (2014).
 [2] Malloy, M. *et al.*, “Massively Parallel E-Beam Inspection: Enabling next-generation patterned defect inspection for wafer and mask manufacturing”. Metrology, Inspection, and Process Control for Microlithography XXIX. Proc. SPIE 9423, 9423-44 (2015) *in press*.
 [3] Kemen, T. *et al.*, “Further advancing the throughput of a multi-beam SEM.” Metrology, Inspection, and Process Control for Microlithography XXIX. Proc. SPIE 9424, 9423-64 (2015) *in press*.
 [4] Bunday, B. *et al.*, “Simulating Massively Parallel Electron Beam Inspection for sub-20 nm Defects”, Metrology, Inspection, and Process Control for Microlithography XXIX, Proc. SPIE 9423, 9424-19 (2015) *in press*.
 [5] This work was supported by SEMATECH

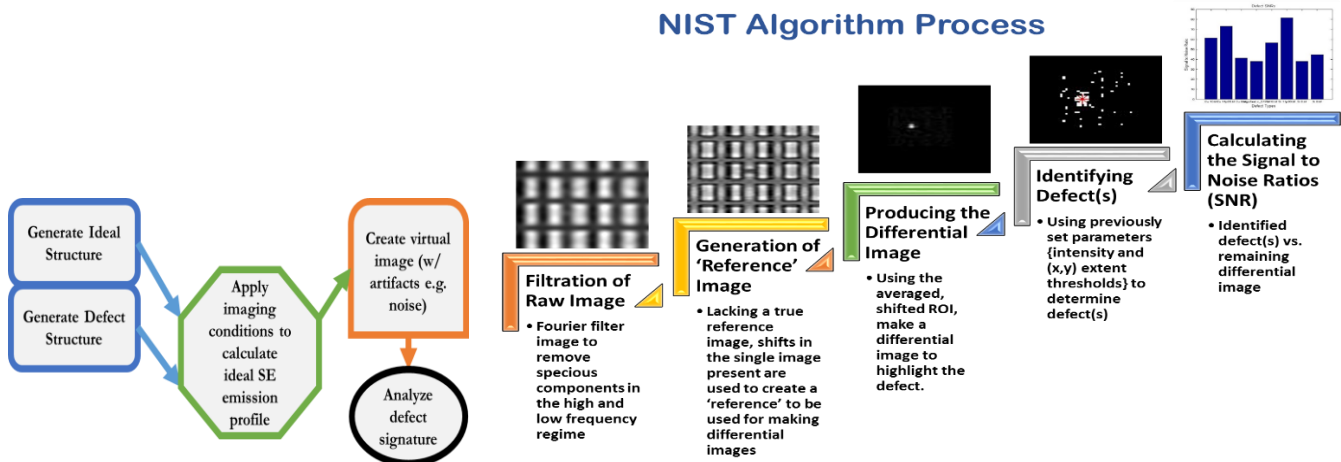


Figure 1. (above left) Flowchart describing the generation of virtual test images
Figure 2. (above right) Flowchart for determining the defect signature strength from images.

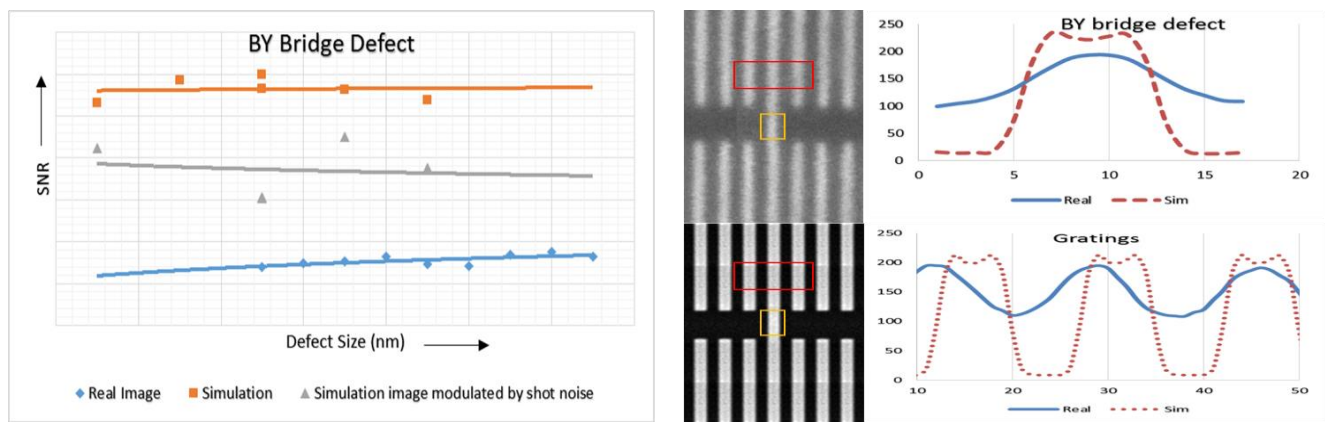


Figure 3. Left – Y-Bridge defect signature strength from simulated image, simulated image modulated by shot noise and real image equivalent. Right – profile plots of the Y-bridge defect in real and simulated mode along with that of a sample size of the intermediate gratings.