

## Performance Metrics For SDD / Digital Pulse Processor Combinations

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Fully characterizing the performance of a Silicon Drift Detector (SDD) and its associated digital pulse processor (DPP) for a particular application requires much more information than the headline resolution and maximum count rate. McCarthy et. al.[1] note that DPP technology improvements have had a significant impact on EDS over the past 15 years. Their role is even more important for SDDs, given the high count rates achievable and the physical differences between SDDs and Lithium-drifted Silicon detectors (Si(Li)s). For example, the variable electron-cloud drift path length, depending on where the X-ray strikes the SDD, results in variable charge integration time in the signal at the preamplifier output as a function of active area and anode/FET location[2].

Therefore, a complete test suite is desirable which considers low-energy sensitivity and peak shape, energy resolution at a range of output count rates, and coincidence (“pile-up”) rejection. The latter is important at high count rates since most SDDs on electron-beam instruments are equipped with light element windows, and coincidence detection is more difficult for low-energy X rays[3].

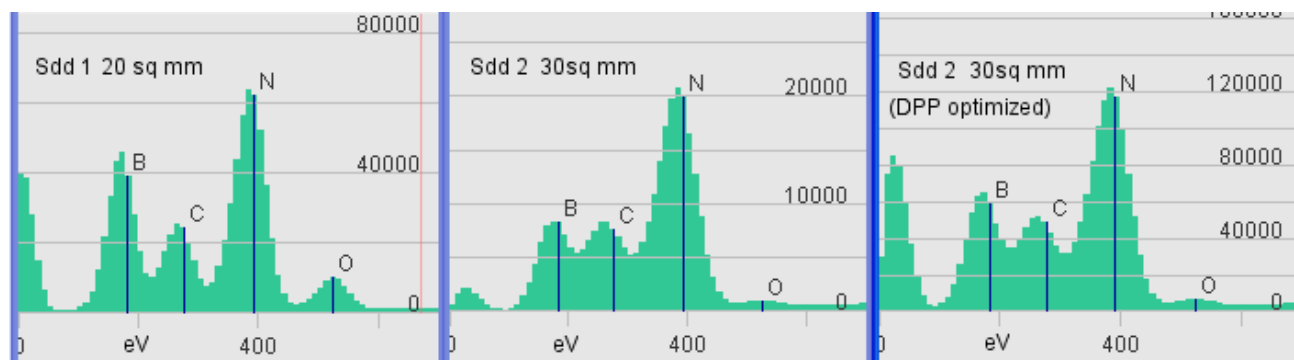
Light element sensitivity and peak shape is a function of SDD surface treatment and DPP settings (Figure 1). The change in resolution with count rate can vary considerably between SDDs from different manufacturers, and between SDDs of different size and type (Table 1).

The ratio of a sum peak to its parent peak or peaks affects detection limits and quantitative accuracy for trace elements which overlap the sum peak. This ratio is only directly comparable between two instruments if the specimen composition, geometry, input count rate and light element transmission are held constant. Statham[3] describes a quantity called Pulse Pair Resolving Time (PPRT) which relates the sum peak area to the input count rate and area of the parent peak or peaks. PPRT is fixed for a given instrument and can be compared for the same energy or energy pair between spectra of different compositions taken under different conditions.

Furthermore, many manufacturers supply software to model and remove the sum peaks from a spectrum. It is important to test the hardware coincidence rejection and the software sum-peak removal separately, since the channel statistics before sum-peak stripping still determine the error limits for an underlying trace peak. Figure 2 shows spectra from the same SDD with different DPPs.

### References

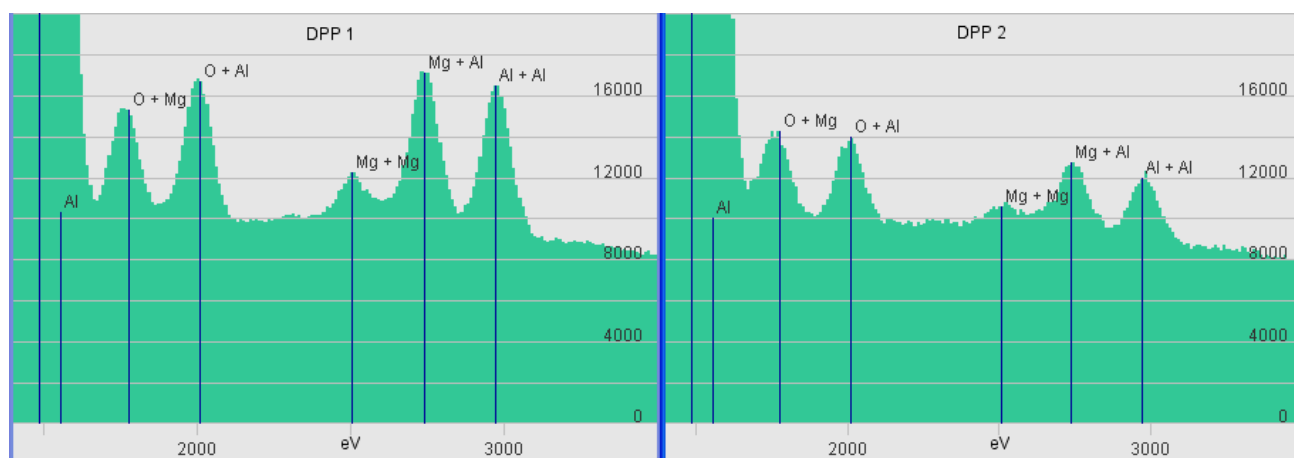
- [1] J. McCarthy, J. Friel and P. Camus, “Impact of 40 Years of Technology Advances on EDS System Performance”, *Microsc. Microanal.* 15 (6) (2009) 484-490.
- [2] <http://www.ketek.net/products/technology.html>
- [3] P. J. Statham, *Microchim. Acta* 155, (2006) 289-294.



**Figure 1.** BN spectra at 5KV from two SDDs. The two spectra from SDD 2 used different DPP edge detection settings. In all cases, the B, C and N peaks are slightly below their theoretical energy. SDD 1 has better B sensitivity than the best DPP setting for SDD 2.

SDD	Description	10kcps OCR	50kcps OCR	200kcps OCR	Notes
A	10 sq. mm. On-chip FET	5% DT 123.5 eV	28% DT 123.6 eV		
B	10 sq. mm. On-chip FET	9% DT 124.6 eV	30% DT 125.7 eV	45% DT 131.5 eV	Mn spectra at 10 KV
C	30 sq. mm. On-chip FET	9% DT 131.5 eV	49% DT 140 eV	50% DT 167 eV	Mn spectra at 25 KV Temperature -30C
D	20 sq. mm. External FET	22% DT 133.7 eV	50% DT 135 eV		20kcps and 36kcps OCR, respectively
E	Older, size unknown External FET	13% DT 145 eV	26% DT 179 eV		Newer external FET devices run colder

**Table 1.** Comparison of energy resolutions for various SDDs at low and high rate.



**Figure 2.** SDD spectrum of Spinel at 35kcps OCR. Two DPPs simultaneously received the same preamplifier signal. Note the difference in sum-peak heights. The spectra have been scaled to match the area of the Al peak.