doi:10.1017/S1431927610057090
Microsc. Microanal. 16 (Suppl 2), 2010

Strain Mapping of 45 nm MOSFET by Dark-Field Inline Electron Holography

V.B. Özdöl*, C.T. Koch* and P.A. van Aken*

* Stuttgart Center for Electron Microscopy, Max Planck Institute for Metals Research, Heisenbergstr. 3, Stuttgart, Germany, D-70569

Strained silicon is now routinely used to enhance the carrier mobility in the latest generation MOSFETs [1]. Although high-resolution transmission electron microscopy (HRTEM) methods [2,3] have shown to provide the required accuracy at the nanometer scale, a much larger field of view is crucial for mapping strain in transistor gate channels. To overcome this, we have lately developed the dark-field inline holography [4] technique. Unlike dark-field off-axis electron holography [5], inline electron holography relies on the reconstruction of the geometric phase from a focal series of dark-field images of 2 non-collinear reflections using a recently developed full-resolution wave reconstruction (FRWR) software [6].

In this contribution, we demonstrate the strain analysis on an array of 45nm MOSFET channels using dark-field inline holography. Fig. 1 shows a bright-field image of a p-MOSFET structure consisting of an embedded SiGe source and drain and a strained Si channel. The longitudinal strain parallel to the gate, ε_{xx}, can be measured from the phase of any of the diffracted beams, scattered along the *x* direction. The geometric phase reconstructed from a focal series of 15 dark-field inline holograms for the (220) reflection is given in Fig 2a. The strain map extracted from the geometric phase combines high spatial resolution, better than 1 nm, with a field of view of about 1 µm in each dimensions.

Its simpler experimental setup, excellent signal-to-noise properties and loose requirements on the spatial coherence are the main advantages of dark-field inline holography. There is also no need for a large reference area of a well oriented crystal specimen, which makes it possible to characterize the strain state of very complicated structures in semiconductor devices.

References

[1] ITRS, International Technology Roadmap for Semiconductors, 2005 edn. Available online at http://www.itrs.net/reports.html.
[2] K. Du, F. Phillipp, *J. Microsc.* 221 (2006) 63.
[3] M. J. Hÿtch, E. Snoeck, and R. Kilaas, *Ultramicrosc.* 74 (1998) 131.
[4] C. T. Koch, V. B. Özdöl, P. A. van Aken, *Appl. Phys. Lett.* (2010) *accepted for publication*.
[5] M. Hÿtch, F. Houdellier, F. Hüe, and E. Snoeck, *Nature* 453 (2008) 1086 109.
[6] C. T. Koch, *Ultramicrosc.* 108 (2008) 141 109.
[7] We acknowledge financial support from the European Union under the FP6 Integrated Infrastructure Initiative, Reference 026019 (ESTEEM).

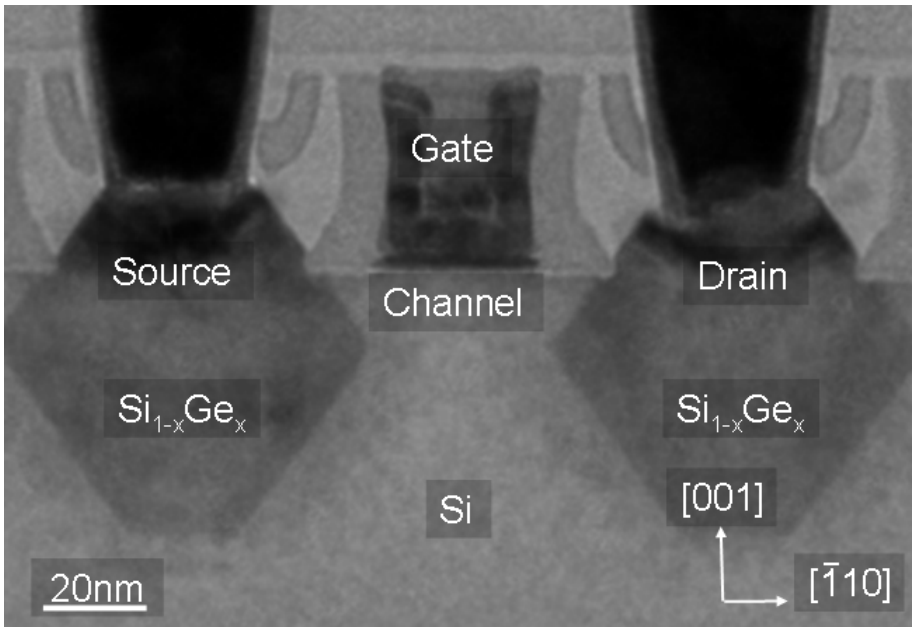

FIG. 1. Bright-field image of the 45 nm technology p-MOSFET structure of a commercial processor. The individual transistor components are labeled.

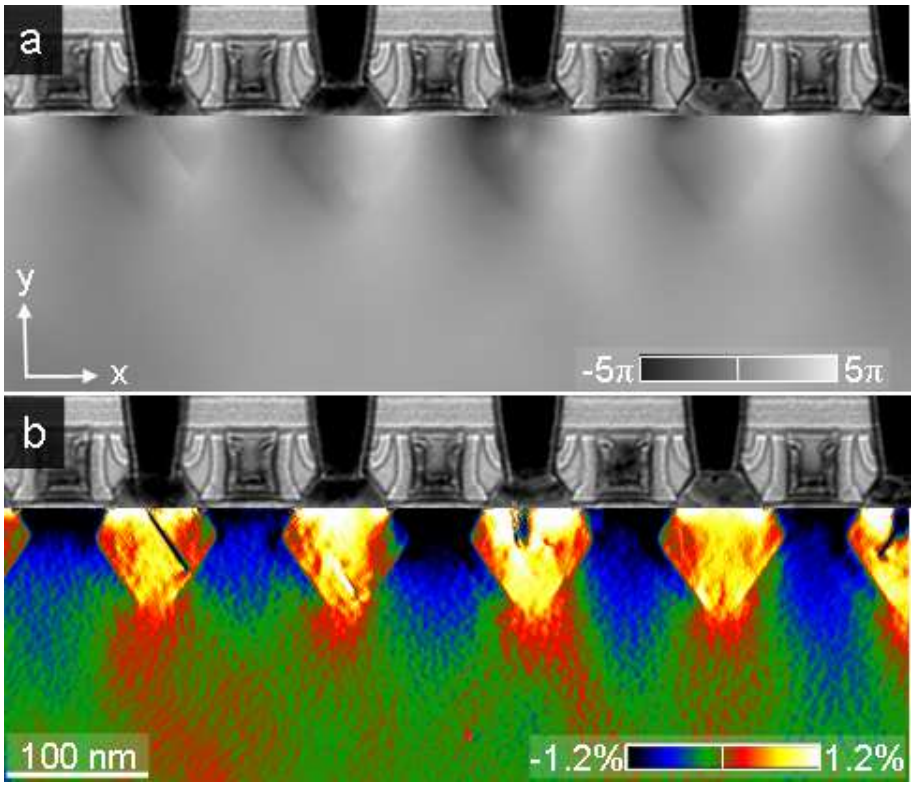

FIG. 2. (a) Geometric phase reconstructed from a focal series of 15 dark-field inline electron holograms for the (220) reflection. (b) Map of the ε_{xx} strain component extracted from the geometric phase map shown in (a). The gate channels are compressively strained. The bright-field image of the contacts is shown on top of the phase image in (a) and the strain map in (b).

https://doi.org/10.1017/S1431927610057090 Published online by Cambridge University Press