doi:10.1017/S1431927610058666
Microsc. Microanal. 16 (Suppl 2), 2010
© Microscopy Society of America 2010

# *In situ* Investigation of Dielectric Breakdown in Field Effect Transistors

C.S. Bonifacio *, A.M. Thron *, G. Bersuker ** and K. van Benthem*

* Department for Chemical Engineering and Materials Science, University of California, Davis, 1 Shields Ave., Davis CA 95616
** International SEMATECH, 2706 Montopolis Dr., Austin TX 78741

Dielectric breakdown of a field-effect transistor occurs when the insulating oxide layer fails to keep the gate capacitance [1]. As a consequence, electron tunneling through the gate dielectric leads to device failure and is inevitable with thinner gate oxides due to device scaling.

Here, we report atomic and electronic structure investigations of a field effect transistor multilayer structure of the form gate electrode/$HfO_2$/$SiO_x$/Si. Although electrical properties and dielectric breakdown mechanisms have been studied before [2,3], only very limited information is available about the evolution of dielectric breakdown and its nucleation sites within individual nanometric device structures. Electrical stress was applied to gate electrodes during *in situ* characterization of the atomic multilayer structure. Experiments were carried out with a double-tilt STM-TEM sample holder (Figure 1). The tip of the scanning tunneling microscope (STM) was used to apply a constant positive bias to the gate electrode while measuring the induced gate current $I_g$ across the gate dielectric. Simultaneously, atomic-scale characterization of the interface structure was performed using a JEOL 2100F/Cs scanning transmission electron microscope.

Figure 1 shows the measured gate current $I_g$ as a function of time. During this first experiment, the gate bias was slowly increased with time from 0V at t=0s to +10V at t=155s. The rapid onset of the gate current indicates dielectric breakdown around +10V. Future experiments will entail the application of a constant gate bias and, hence, the observation of time-dependent dielectric breakdown. Figure 2a and b show TEM micrographs of the observed multilayers *prior* and *post* dielectric breakdown, respectively. The TEM provides nanometer precision positioning of the STM tip on the gate electrode of the field effect transistor (Figure 2c). We currently conduct HRTEM, aberration-corrected STEM and STEM-EELS characterization of the interface structure before, during and after dielectric breakdown.

During the presentation, we will report *in situ* observations of time-dependent dielectric breakdown, i.e. the evolution of the atomic and electronic interface structures under applied electrical stress.

[1] R. Waser, *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*. 2nd Edition, Germany, 2005.
[2] G. Bersuker et al., *IEDM Tech. Dig.* (2008)
[3] X. Li et al., *IEDM Tech. Dig.* (2008)
[4] The authors acknowledge financial support through start-up funds from the University of California at Davis. Technical assistance by Dr. Junhang Luo of Nanofactory during the initial STM-TEM experiments is appreciated. Parts of this research were carried out at the National Center for Electron Microscopy (NCEM) at Lawrence Berkeley National Laboratory.

https://doi.org/10.1017/S1431927610058666 Published online by Cambridge University Press

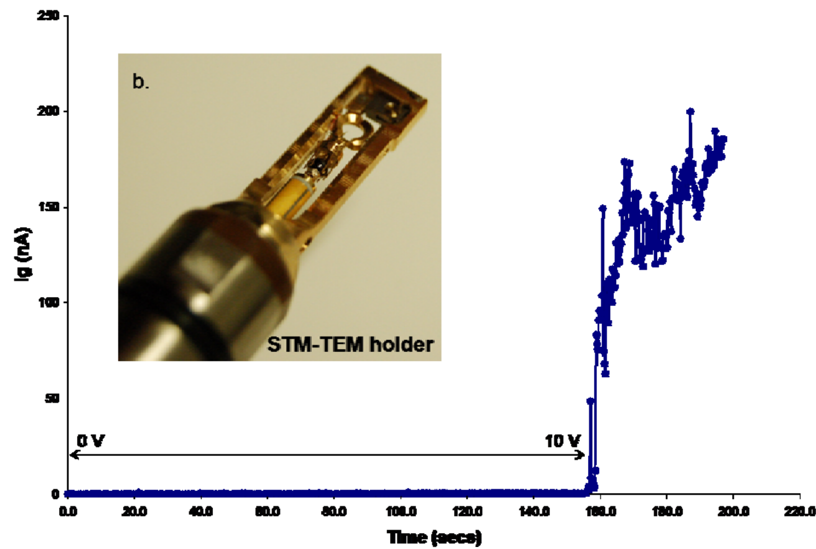


Figure 1. Evolution of dielectric oxide degradation with breakdown of the 3 nm $HfO_2$ gate oxide occurring at a gate bias of +10 V. Inset: image of the Nanofactory double-tilt STM-TEM specimen holder with the STM tip allowing local application of bias directly to the gate electrode.

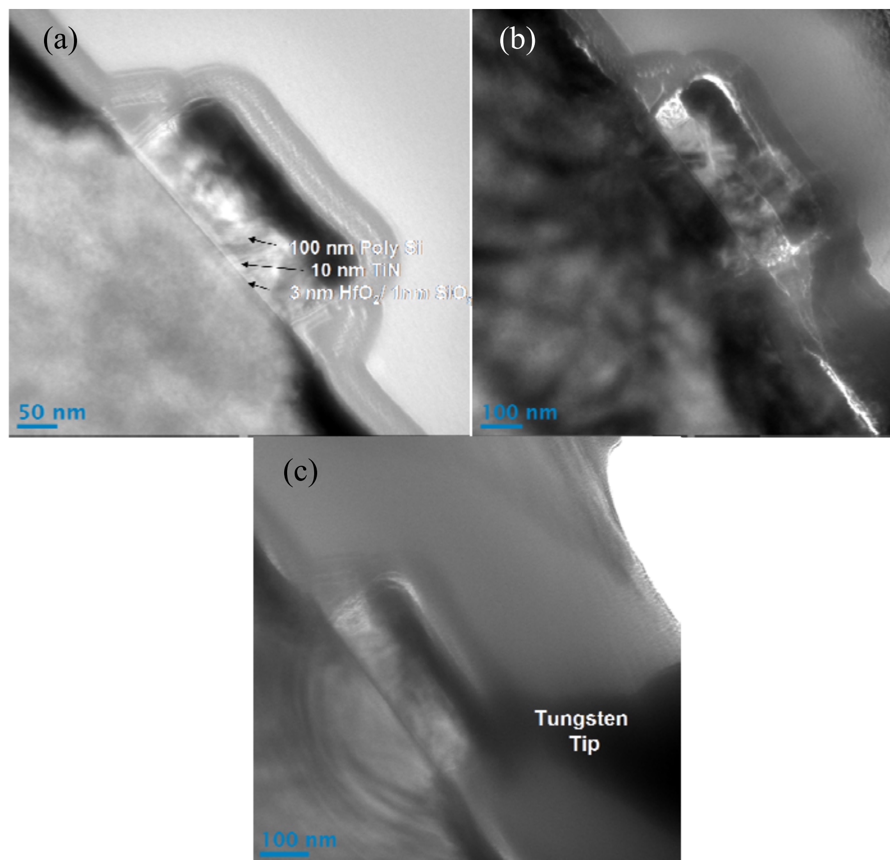


Figure 2. Cross-sectional TEM micrographs of the field effect transistor (100 nm Poly-Si and 10 nm TiN)/3 nm $HfO_2$/ 1 nm $SiO_x$) before (a) and after (b) dielectric breakdown. (c) shows the STM tungsten tip precisely placed in contact to the 100 nm Poly-Si gate electrode.

https://doi.org/10.1017/S1431927610058666 Published online by Cambridge University Press