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High Energy BSE/SE/STEM Imaging of 8 um Thick Semiconductor Interconnects

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High energy (100-400 keV) scanning electron microscope (SEM) imaging of samples can be performed in the transmission electron microscope (TEM)/scanning TEM (STEM) when the system has secondary electron (SE) and/or backscattered (BSE) electron detector(s) installed. Previously, very high resolution SE imaging has been demonstrated at 200 keV in a STEM with a spherical aberration corrected condenser lens [1]. Additionally, imaging of semiconductor Cu interconnects in SiO2 dielectric located at distances > 3um below the surface has been accomplished using incident beam energies of 100-400 keV and a backscattered electron (BSE) detector [2]. In the high energy BSE analysis case, multilevel Cu interconnects are ideal structures to study because: 1) there is a large BSE yield difference between Cu and SiO_2 so Cu can be easily detected and 2) Cu lines exist at multiple levels below the surface so multiple structures can be seen from different depths in one BSE image. In this paper, a semiconductor chip with 9 interconnect levels spanning 8 um in height was studied using SE, BSE and STEM imaging at incident beam energies of 300-400 keV in order to understand image content and quality versus the depth of the structure below the surface.

A 90 nm technology semiconductor chip with 9 interconnect levels was prepared for imaging in a JEOL 4000-FX 400 keV LaB6 TEM/STEM by first mechanically polishing the backside of the chip and then mounting it on an open brass frame using epoxy. The chip was partially masked using lithography tape and Si was completely etched off an unmasked region on the chip using XeF_2 gas. An SE image of the chip taken from the backside is shown in Fig. 1 post XeF_2 etch. To record SEM images, the JEOL 4000-FX system has an in-lens Everhart-Thornley SE electron detector and a semiconductor BSE detector and STEM images were recorded using bright field (BF) and dark field (DF) optically coupled scintillator detectors. A TEM cross-section image of the chip's interconnect structure is shown in Fig. 2.

The chip was initially imaged from the backside, see Fig. 3 a)-c) for 400 keV backside SE, BSE and BFSTEM images, respectively, and then the same region was imaged from the topside, see Fig. 3 d)-f) for 400 keV topside SE, BSE and BF-STEM images, respectively. The backside SE image shows surface details such as regions that were etched by XeF_2 and contamination on the sample surface. The backside BSE image has no surface detail but sub-surface W vias and Cu lines are seen. Though the beam penetrated through 8 um of material, a decent resolution BF-STEM image from the upper levels of the sample was acquired and the contrast is similar to the BSE image but inverted. The topside BSE and BF-STEM images differed significantly from the backside images, e.g. the W vias clearly seen from the back were not visible from the top. Cu/W can be detected ~4 um below the surface and all of the 8 Cu line levels can be imaged by 400 keV BSE or BF-STEM when images are taken from both back and top sides.

References:

[1] Y. Zhu, H. Inada, K. Nakamura and J. Wall, Nature Materials, **8**, 808 (2009).
[2] L.M. Gignac, M. Kawasaki, S.H. Boettcher and O.C. Wells, J. Appl. Phys., **97**, 114506 (2005).

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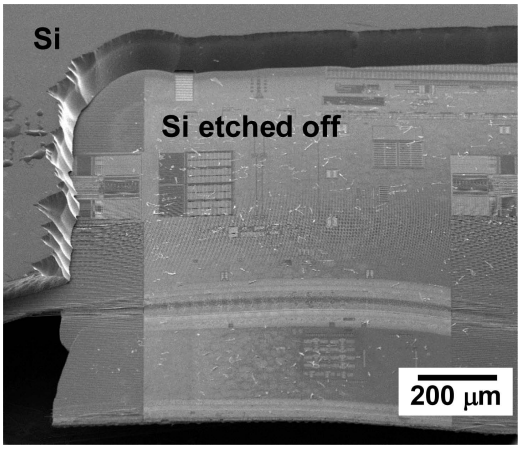

Figure 1 (above): 5 keV SE image of the back-side of the chip showing the Si etched region.

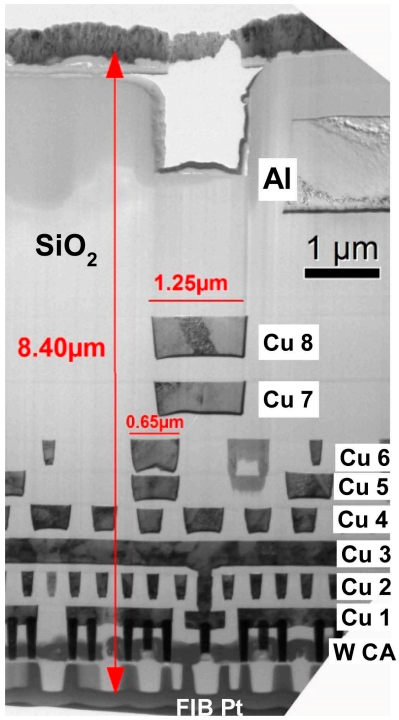

Figure 2 (left): TEM cross-section image of chip's 9- level interconnect structure.

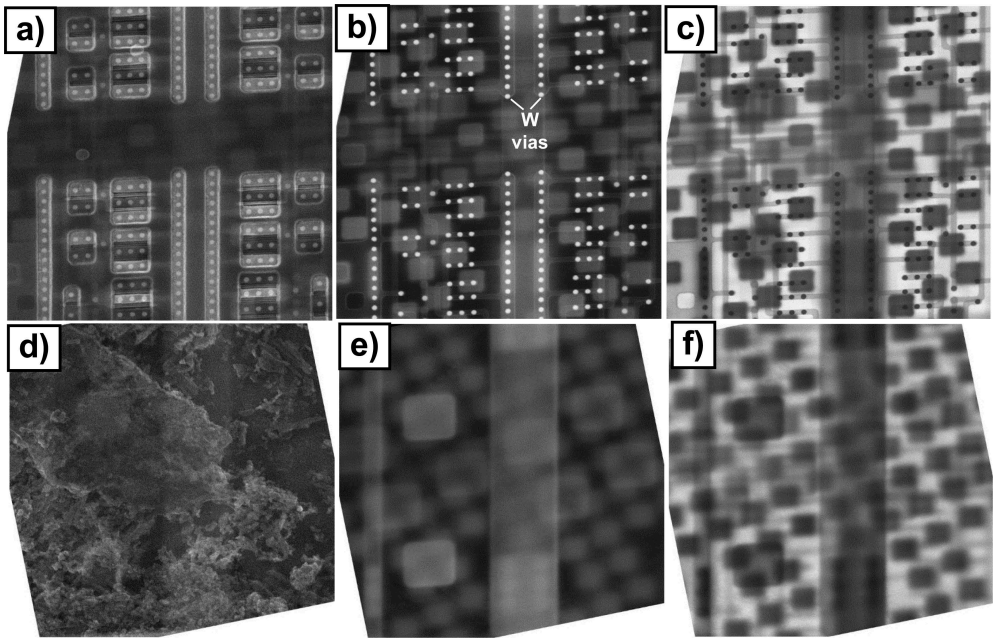

Figure 3: 400 keV images of the same region on the chip taken from the backside: a) SE, b) BSE, c) STEM and the topside: d) SE, e) BSE, f) STEM.

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