Sample preparation for aberration-corrected microscopy of high-quality TEM specimens of advanced integrated circuits

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Advanced integrated circuits (ICs) are complex due to the fin field effect transistors (FinFETs), which comprise multigate transistors with the source/drain (S/D) channels (fins) surrounded by a three-dimensional gate. State-of-the-art ICs are at the 10 nm and 7 nm nodes, with the later at the ramping stage of production[1]. At the 10 nm node, the S/D fins are 25% taller and 25% more closely spaced than 14 nm node technology [2]. Transmission electron microscopy (TEM) is a critical characterization tool for the semiconductor industry given the decreasing device size. Ga $^+$ focused ion beam (FIB) is frequently used for advanced IC TEM specimen preparation due to its rapid, site-specific sample preparation capabilities. However, FIB milling typically results in specimen artifacts, such as surface amorphization and Ga $^+$ implanted layers, both of which may limit analytical and high-resolution electron microscopy. Furthermore, 20 nm or less specimen thickness is required to characterize the 3D structures of the FinFET gate oxide in the TEM [3]. In this work, we present targeted, small spot (< 1µm), low energy Ar $^+$ milling for reproducible specimen preparation of advanced ICs with specimen thicknesses of less than 20 nm that removes FIB-induced artifacts.

An Intel Broadwell M core processor was deprocessed and from it a cross-section specimen was created using the inverted method in a dual-beam FIB [Thermo Fisher]. Following 5 kV milling in the FIB, specimen thicknesses that ranged from 80 nm to 200 nm were obtained. An ion milling system [Fischione Instruments] was used to iteratively mill the specimens at decreasing energies (from 900 to 500 eV). TEM and scanning TEM (STEM) characterization were performed before and after each ion milling step (the specimen was mounted on a TEM specimen holder that is compatible with both the Ar⁺ ion mill and the TEM goniometer). Specimen thickness was determined by electron energy loss spectroscopy (EELS). The specimens were further imaged in a probe-corrected ARM200F [JEOL] after ion milling.

Preliminary results after ion milling resulted in electron-transparent specimens, as shown by the aberration-corrected dark field (DF) and bright field (BF) STEM images in Figures 1a-b, respectively. In Figures 1a-b, the atomic columns of Si in the fin and amorphous high-k (dark layer in DF-STEM; bright layer in BF-STEM) and work function setting material (bright layer in DF-STEM; dark layer in BF-STEM) above the fin were easily identified. EELS energy-filtered TEM (EFTEM) results (Figures 1c-d) indicated t/λ ranging from 0.22 to 0.11, which are equivalent to specimen thicknesses of 32.6 to 16.3 nm. To confirm reproducibility, another set of specimens was iteratively milled by the Ar⁺ milling system using the same parameters. The removal of the layers across the fin structure was determined by tilting the specimen in the TEM and acquiring DF-STEM images in between milling steps. Figure 2 shows the layer-by-layer removal across the fin structure – namely the gate oxide, spacer, and metal interconnects. The fin structure of the FinFET was targeted until the gate-oxide layers on both sides of the specimen were revealed (Figure 2c). Aberration-corrected microscopy and EELS thickness analysis are underway.

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References:

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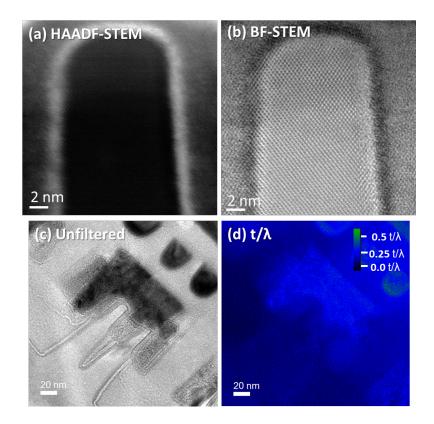


Figure 1. Aberration-corrected, high-angle, annular dark field (a) and bright field (b) STEM images of the FinFET structure after ion milling. Specimen thickness was calculated to be 25.2 nm based on a MFP=148.121 nm and t/λ =0.17 derived from the unfiltered image (c) and EFTEM thickness map (d). The color is based on the t/λ scale.

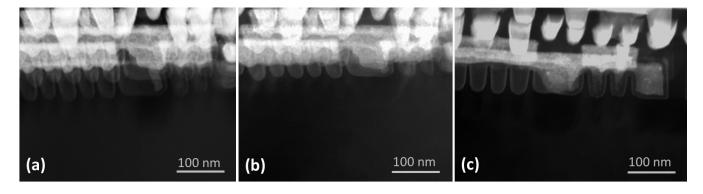


Figure 2. HAADF-STEM images of the specimen tilted at $\pm 27^{\circ}$ before Ar⁺ milling (a) and following 700 eV (b) and 500 eV (c) Ar⁺ milling. The gate oxide, spacer, and metal interconnect layers across the fin structure were removed layer-by-layer.