

Position and Energy Resolved Room Temperature X-ray Detectors

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Two dimensional arrays of silicon X-ray detectors have been developed since many years. In order to reach Fano limited energy resolution they required cooling down to -100°C or less. They were either based on conventional CCD concepts, derived from the devices originally developed for optical applications. Or they were composed by Si(Li) or Ge detector elements with coarse position resolution. Under those conditions every pixel must be connected to a readout chain. Most recently, a big step forward towards (close to) room temperature operation of up to $500\ \mu\text{m}$ thick depleted back illuminated active pixel sensors and frame store pnCCDs was made. Both device types are derived from the concept of sideward depletion – the underlying principle of silicon drift detectors. A dedicated fabrication process and the high speed operation of the new detectors, (e.g. up to 1000 frames per second at a format of 64×64 and 256×256 with a pixel size of $75\times 75\ \mu\text{m}^2$) were yielding energy resolutions at the Mn K α line at 5.9 keV of 140 eV (FWHM) at an operation temperature of -10°C only. This operation allows for position resolved high count rate spectroscopy easily achievable with thermoelectric coolers. In the preliminary analysis of the data, the peak to background was 1000:1. This is mainly due to the not yet optimized pattern analysis of the photon events distributed over more than one pixel and the unification of othe split events.

One of the detector types under study is an active pixel sensor based on the DEPFET principle. (see Fig. 1 and 2) The electronic noise contribution of the DEPFET amplifier is 2.2 electrons (rms) at room temperature. The resulting spectroscopic performance is dominated by thermally generated leakage currents, typically 100 pA per cm^2 at full depletion of $450\ \mu\text{m}$. Spectra at various operational conditions will be shown to define the bandwidth of specific applications.

- At room temperature $T=22^{\circ}\text{C}$, $\Delta E = 200\ \text{eV}$ (FWHM)
- At $T= -10^{\circ}\text{C}$, $\Delta E = 140\ \text{eV}$ (FWHM)
- At $T= -30^{\circ}\text{C}$, $\Delta E = 130\ \text{eV}$ (FWHM)

A second detector type, the frame store pnCCD, will be briefly described. The reliability and robustness of this class of devices will be highlighted through applications in heaven and on earth. They have shown good energy resolution as well: $\Delta E = 145\ \text{eV}$ (FWHM) at 0°C with a 256×256 large $4\ \text{cm}^2$ large device with 400 frames per second readout speed.

The system configuration of both detector types, including the ASIC frontend electronics will be introduced to demonstrate the compactness and the the low power operations of the systems.

The sensitivity for X-rays is excellent: The high quantum efficiency ranges from 70 eV (90%) to 13 keV (90%). Electrons can be imaged directly up to energies of 1 MeV, the radiation hardness for the back illuminated devices is extremely high, only limited by the leakage current generated through the

damage. The measured damage relates to a current increase of 10^{-17} A per minimum ionizing particle going through the detector volume.

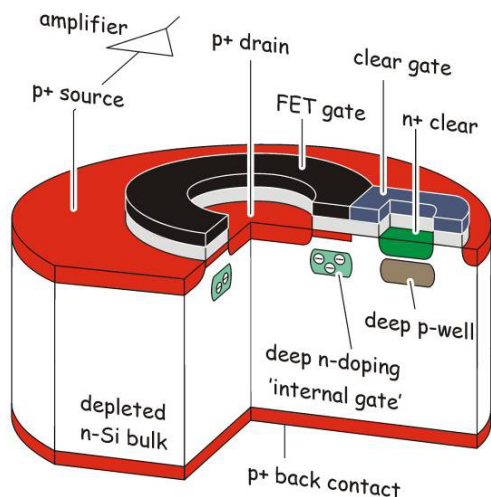


Fig.1. Schematic view on a depleted p-channel FET (DEPFET). A drain contact in the center is surrounded by a MOS gate structure, again surrounded by a source contact. Underneath the gate a potential minimum for electrons is located, collecting all charges generated within the detector volume. Every electron in the internal gate gives rise to an increase of the FET current by typically 1 nA. This increase in current can be easily measured. The "green" contact on the right hand side serves as a clear contact of the charges from the internal gate.

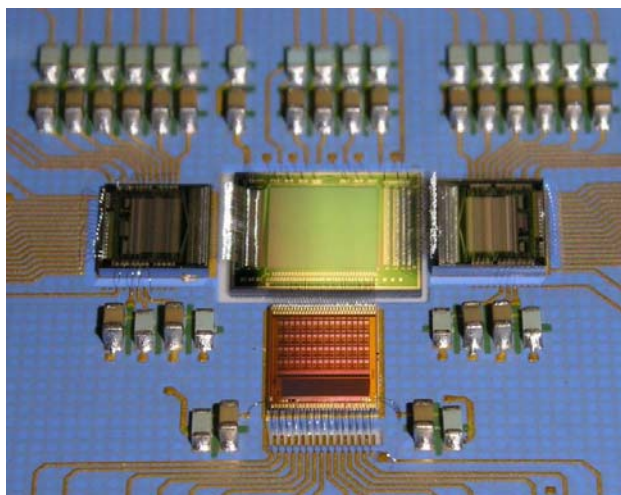


Fig.2. Photograph of the active pixel sensor system. The DEPFET matrix is in the center (64×64 pixel of $75 \times 75 \mu\text{m}^2$). The ASIC on the left side selects the rows to be read out, the chip on the right side addresses the clear voltages to the selected rows. The ASIC below is a 64 channel signal processor for the low noise amplification of the on-chip preamplified signals. It comprises a selectable gain within a range of 1.000. The highest gain stage operates from 100 eV to 10 keV, the lowest gain from 10 keV to 1 MeV.

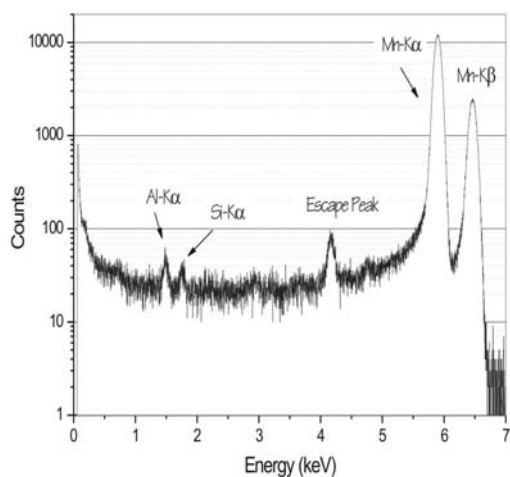


Fig. 3. ^{55}Fe spectrum recorded with the DEPFET active pixel sensor at -30°C . The FWHM of the Mn K α line is 130 eV only. The peak to background ratio is 1.000:1, limited by not yet optimized analysis software. As in the pnCCD case we expect a P/V ratio of 6.000:1. The measured position resolution for X-rays is below $10 \mu\text{m}$.