Characterization of 6H-SiC/SiO₂ Interfaces by EFTEM Elemental Mapping

J. Bentley,* K.-C. Chang,^{$\ddagger §$} and L.M. Porter^{\ddagger}

*Metals & Ceramics Div., Oak Ridge National Laboratory, PO Box 2008, Oak Ridge, TN 37831-6064 *Department of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA 15213 *Now at: Seagate Technology, 2403 Sidney Street, Suite 550 Pittsburgh, PA 15203

The ability to easily form an SiO₂ dielectric layer is an important aspect of the dominance of silicon in microelectronics. An SiO₂ layer is also easily formed by oxidation of SiC in oxygen or steam. SiC devices have the potential for faster switching speeds, higher voltages, smaller size, lower power losses, higher temperatures and less cooling. However, interface-state densities D_{it} (cm⁻²eV⁻¹) are high (10¹¹ to 10¹³ for SiC/SiO₂; c.f. ~ 5 x 10⁹ for Si/SiO₂) and channel mobilities are low. A contributing reason for the inferior properties of the SiC/SiO₂ interface is believed to be the presence of carbon as a byproduct of the oxidation process. A number of post-oxidation annealing procedures have been used to improve the quality of the interface. A re-oxidation step at 950°C has commonly been employed to reduce D_{it} , with the mechanism believed to be associated with removal of C trapped at the interface during the oxidation process.

Elemental mapping by energy-filtered transmission electron microscopy (EFTEM) has been used to measure compositions at the SiC/SiO₂ interface for various processing conditions. The material was 6H-SiC (0001) from Cree, Inc. having an n-type epilayer with a doping concentration of 1 x 10^{16} cm⁻³. Following standard RCA cleaning, with or without sacrificial oxidation, oxidation was performed for 4 h at 1100°C, or for 4 h at 1100°C plus a re-oxidation for 3 h at 950°C, or for 12 h at 950°C. A thin layer of Cr was deposited at room temperature to protect the oxide surface and crosssection TEM specimens were prepared by conventional grinding and ion milling procedures. EFTEM was performed with a Philips CM30 (LaB₆ cathode) and Gatan imaging filter (GIF). An incident beam convergence $\alpha = 2.6$ mrad, collection semi-angle $\beta = 4.8$ mrad, 2x binning (512² pixels) with 0.32-nm pixels, 3-window mapping with AE^{-r} background fitting, and custom Digital Micrograph scripts for image alignment were used. For SiL₂₃, 10-eV windows (Δ) centered at 78, 88 and 118 eV and 3-s exposures were used; 20-eV windows and 15-s exposures were used for C (248, 268 and 294 eV) and O (497, 517 and 543 eV). Incident illumination was constant for the 9 core-loss images of a given area. Specimens were tilted so that s_g>0 for g=00012 to avoid strong diffraction contrast effects. Figure 1 shows C, O, and Si maps (net core-loss intensities) for a sample oxidized 4 h at 1100°C. Also included are (C map)/(Si map), (O map)/(Si map), and a map of $t/\lambda = \ln(\text{unfiltered/zero})$ loss), where t is specimen thickness and λ is the inelastic scattering mean free path. The diffraction contrast in the Cr layer was critical in performing image alignment among the 9 core-loss images. Quantitative compositions were obtained from the elemental maps, calculated partial ionization cross-sections $\sigma(\Delta,\beta)$, and exposure times T; e.g., C/Si = (C map)/(Si map).(σ_{Si}/σ_{C}).(T_{Si}/T_{C}). Quantitative composition profiles normal to the SiC/SiO₂ interface were extracted with the DigitalMicrograph profile tool. Profiles were averaged over 100 pixels (32 nm) parallel to the interface to reduce noise. Results for 6H-SiC oxidized 4 h at 1100°C, with and without sacrificial oxidation in the cleaning stage, are shown in Figure 2. In some, but not all, regions there is a pronounced maximum in the C/Si atomic ratio at the SiC side of the interface, indicating the presence of excess C. The largest maxima correspond to ~2 monolayers of C. Typical profiles for 6H-SiC oxidized for 4 h at 1100°C and re-oxidized 3 h at 950°C are shown in Figure 3. Again some, but not all, regions exhibit excess C (but not as much as in specimens without the additional 3 h at 950°C). For 6H-SiC oxidized 12 h at 950°C no excess C was detected along the interface. D_{it} values at 0.4 eV below the top of the band gap are 1.8, 1.02 and 0.70 x 10¹² eV⁻¹ cm⁻² for 6H-SiC oxidized at 1100, 1100 + 950, and 950°C, respectively, and thus seem to correlate with the level of excess C. Extensions of this research involve 4H-SiC metal-oxide-semiconductor field-effect-transistors (MOSFETs) [2,3].

1. K.-C. Chang, J. Bentley and L.M. Porter, J. Electronic Materials 32 (2003) 464-9.

2. K.-C. Chang, L.M. Porter, J. Bentley, C.-Y. Lu and J. Cooper, Jr., J. Appl. Phys. 95 (2004) 8252.

3. Financial support from the Office of Naval Research via ONR Award No. N00014-02-1-0628 is gratefully acknowledged (KCC, LMP). Research at the ORNL SHaRE User Facility (JB) sponsored by the Division of Materials Sciences and Engineering, Office of Basic Energy Sciences, U.S. Department of Energy, under contract DE-AC05-000R22725 with UT-Battelle, LLC.



FIG. 1. EFTEM elemental mapping of 6H-SiC oxidized 4 h at 1100°C. See text for details.



FIG. 2. C/Si atomic ratio profiles across SiC/SiO_2 interface after oxidation at 1100°C for 4 h. Note excess interfacial C in regions 1,2 and 5.



