

A Next Generation Electron Microscopy Detector Aimed at Enabling New Scanning Diffraction Techniques and Online Data Reconstruction

Ian J. Johnson¹, Karen C. Bustillo², Jim Ciston², Brent R. Draney³, Peter Ercius², Erin Fong¹, Azriel Goldschmidt¹, John M. Joseph¹, Jason R. Lee³, Andrew M. Minor², Colin Ophus², Ashwin Selvarajan³, David E. Skinner³, Thorsten Stezelberger¹, Craig S. Tindall¹ and Peter Denes⁴

¹. Engineering Division, Lawrence Berkeley National Laboratory, Berkeley, California, USA

². National Center for Electron Microscopy, Molecular Foundry, Lawrence Berkeley National Laboratory, Berkeley, California, USA

³. National Energy Research Scientific Computing Center, Berkeley, California, USA

⁴. Physical Sciences, Lawrence Berkeley National Laboratory, Berkeley, California, USA

Advancements in detector technology have enabled the innovation of new scientific methods in electron microscopy. In traditional scanning transmission electron microscopy (STEM) current detector technologies either capture only a few measurement values per probe position or are frame rate limited to about 1 kHz which restricts the electron beam scanning speed and or granularity of the resulting STEM image. This new detector system consists of a central pixel detector and outer annular rings that record signals at close to 100k frames per second. It provides the capability to simultaneously acquire the information rich convergent beam electron diffraction (CBED) pattern and High Angle Annular Dark Field (HAADF) signal at every electron beam position on the sample at speeds that approach the limitation of the electron beam steering scan coils. This is an end-to-end development which encompasses the detector, data transportation and real-time data processing. A combination of in-hardware edge-computing at the source, high-bandwidth (400 Gbps) data transfer directly into the memory of a supercomputer, and online data processing on the Cori supercomputer [1] will provide prompt experimental feedback.

Initial experiments with this new detector will combine the CBED data from the central pixel detector and the HAADF signal from surrounding circular diodes to obtain a deeper understanding of the sample at every raster scan position. The central diffraction pattern reveals information about structure, composition, polarization and three-dimensional defect crystallography. The HAADF signal complements these measurements by assessing the mass-thickness contrast of the sample. This detector will be installed on the Transmission Electron Aberration-corrected Microscope (TEAM) [2].

One key component to advancements in transmission electron microscopy over the last 10 years has been the utilization of direct electron detectors, such as the one developed for TEAM I [3]. CMOS Active Pixel Sensors (APS) used in TEM have small pixels that provide single electron sensitivity. This new sensor consists of a 576 x 576 array of 10 μm pixels and an outer HAADF detector with 16 concentric quadrants diodes (64 elements). Digitized data from these sensors will be sent over 96 multi-gigabit optical links to 4 Field Programmable Gate Array (FPGA) modules. Ultimately, in-FPGA data reduction will reduce the overall data bandwidth, but for initial use, all data will be transported via a 400 Gbps optical link to the National Energy Research Scientific Computing Center (NERSC). The 400 Gbps bandwidth will limit the initial frame rate to 75 kHz, and higher rates will be obtained with data reduction on the detector.

In-hardware edge-computing will carry out the first stage of data processing before the data is placed on the network. Image reconstruction through the reorganizing of pixels into the CPU preferred (x,y)

coordinates and calibrations like dark noise subtraction will be implemented on hardware in FPGAs. Standard STEM image reconstructions like the integrated intensity of the bright and dark field signals as a function of scan position will also be calculated at the detector in firmware and provide instantaneous feedback to the scientists. Placing more resource intensive data processing and reduction algorithms in the firmware, like single electron cluster finding and more complex real-time data analysis, will also be investigated. The data acquisition FPGA modules will communicate the basic STEM images over a low bandwidth online display channel, and the preprocessed data over the high-bandwidth, 400 Gbps, 1 km link to the Cori supercomputer at NERSC. The former channel provides real-time feedback for sample alignment, while the latter is utilized for in-depth data analysis.

Data receiver batch jobs on Cori will receive complete image sets from the FPGA modules and pass them on to processes that conduct online analysis and store the data. By design this is a parallel computational architecture, in which throughput scales with the number of jobs. Compression factors of more than 100 are expected when analog signals from the detector are converted to electron events, "electron counting". After data reduction, complete data sets will be handed to a HDF5 file writer and will also be available for online analysis routines. Our goal is to have prompt feedback from more complex analyses, like phase contrast imaging methods such as Matched Illumination and Detector Interferometry (MIDI) [4] and ptychography [5, 6].

References:

- [1] <http://www.nersc.gov/users/computational-systems/cori>
- [2] C. Kisielowski et al., *Microscopy and Microanalysis*, **14** no. 5 (2008), p. 469.
- [3] M. Battaglia, et al., *Nucl. Inst. and Methods in Phys. Res. A*, **622** no. 3 (2010), p. 669.
- [4] C. Ophus et al., *Nat. Comm.* **7** (2016), p. 10719.
- [5] Y Jiang et al., arXiv:1801.04630 (2018).
- [6] This work was supported by the Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. Research was performed at the Molecular Foundry and the National Energy Research Scientific Computing Center, DOE Office of Science User Facilities.

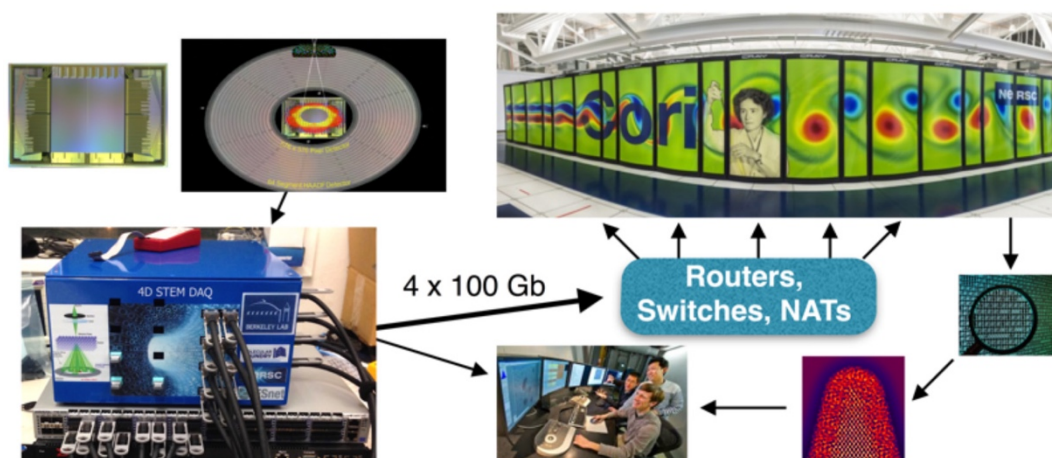


Figure 1. Illustration of the detector system and data path to analysis. Starting in the upper left and following the data path: CMOS APS sensor and annular HAADF diodes, FPGA based data acquisition system, 400 Gbps network, Cori supercomputer at NERSC, prompt and real-time feedback to the users.