capacitively coupled with the input voltage V_i through an 8-nm-thick Al_xO_y layer. Small tunnel junctions connect the transistors to power lead, output, and ground. A load capacitor connects the output to the ground to suppress charging effects. Two tuning gates, with voltages V_{g1} and V_{g2}, are used to tune the induced charges on the two islands.

The device was fabricated on a thermally oxidized silicon substrate using a high-resolution electron-beam pattern generator at 100 kV. A bottom layer of Al served as the lower electrodes of the gate capacitors and the load capacitor. An Al_xO_y dielectric layer was created upon these electrodes by oxidizing the sample in an O_2 plasma. A second (upper) layer of Al forms the aluminum islands and the leads; on this layer the four tunnel junctions were defined by shadow evaporation.

The inverter operates such that one SET is conducting while the other is in Coulomb blockade, depending upon the input voltage. Shifting the input voltage alters the induced charge on the SETs by a fraction of an electron and inverts the input.

Measurements were performed in a dilution refrigerator with a base temperature of 25 mK, while suppressing superconductivity using a 1 T magnetic field. The input–output behavior of this device varied greatly depending on the two gate voltages V_{g1} and V_{g2}. A maximum voltage gain of 2.6 was achieved at 25 mK, which remained larger than one up to about 140 mK, confirming that the device operated as designed. This is the highest temperature for which voltage gain in a SET has been achieved.

Inverters are building blocks for other digital logic elements, including NAND or NOR gates, SRAMS, and ring oscillators which should be producible from variations of or combinations of SET inverters. To date, however, there is no automatic method that would allow optimization of performance by adjusting gate voltages on-chip. The researchers state that "this is probably the largest problem inhibiting the further development of this sort of logic."

WIRAWAN PURWANTO

Electrophoretic Approach Results in 3D Assemblies of Gold Nanoparticles

A promising synthetic path for the preparation of three-dimensional (3D) films of gold nanoparticles has been described by a team of researchers at the Notre Dame Radiation Laboratory. In the February issue of *Nano Letters*, they report that highly porous nanostructured films were assembled using an electrophoretic approach. The film thickness could be controlled by varying the concentration of gold colloids in solution and the applied voltage. The particles did not aggregate, as evidenced by the strong surface plasmon band.

The electrophoretic deposition method subjects colloidal solutions of tetraoctylammonium-bromide-capped gold nanoparticles of 5–10-nm diameter in toluene to a dc electric field (50–400 V). This results in a negative charge on the gold nanoparticles, which are then driven toward the positively charged electrode surface. In this study, the composite electrode consisted of an optically transparent electrode (conducting glass) onto which was cast a nanostructured TiO_2 film. The porous TiO_2 film is required for good deposition of the gold nanoparticles. The nanoparticles form a 3D array on the electrode surface without undergoing aggregation or inducing bulk film effects.

"We believe that the capping material acts as a spacer between the adjacent particles in the film," said senior research scientist Prashant V. Kamat, who conducted this study together with Nirmala Chandrasekharan, a postdoctoral researcher at the Radiation Laboratory. "The films exhibit a strong surface plasmon band, which indicates that they retain their identity as individual nanoparticles." The thickness of the films can be controlled by adjusting the concentration of the colloidal solutions and the applied voltage.

The nanostructured films obtained by electrophoretic deposition are stable in atmosphere and highly porous, thus providing a large surface area for anchoring electroactive or photoactive molecules.

"To the best of our knowledge, this is the first report that highlights the feasibility of achieving relatively thick nanoporous gold films with minimal aggregation effects," said Kamat. "The ability to assemble gold nanoparticles as a 3D array of clusters opens new avenues for designing sensors and optoelectronic nanodevices. Nanostructured gold films of high surface area also have potential applications in catalysis and photoelectrochemistry."

CORA LIND

Self-Interstitial Clusters Diffuse Extremely Fast in Crystalline Silicon

Theoretical studies of the self-interstitial defect I in crystalline silicon show that

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