CONFERENCE REPORT

Advanced Metallization Conference 2001 Held in October

The Advanced Metallization Conference 2001 (AMC2001), chaired by Andrew J. McKerrow (Texas Instruments, Inc.) and Yosi Shacham-Diamand (Tel Aviv University), was held October 7–10 at the Queen Elizabeth Hotel in Montreal. About 145 attendees were offered 30 oral and 70 poster presentations, with 11 invited speakers, including a keynote speech by David Harame of IBM Microelectronics. The conference was preceded by two tutorials organized by Bob Blewer (Sandia National Laboratories). The first tutorial was a review of copper/low-*k* unit processes for manufacturing, while the second tutorial focused on characterization techniques for ultralow-*k* dielectric films.

New to AMC2001 was a session on vertical integration, organized by T. Cale (Rensselaer Polytechnic Institute). Papers presented in this session identified the synergy between metallization concerns for on-chip and chip-to-chip interconnects. For example, the talk on "InterChip Via Technology by Using Copper for Vertical System Integration" by researchers from the Fraunhofer Institute for Reliability and Microintegration, Munich, Germany, and Chemnitz University of Technology detailed a viable chip-to-chip Cu interconnect (shown in Figure 1). Six papers were included in this session, including work by IBM, Intel, Tohuko University, and RPI and the State University of New York.

The process-integration sessions included presentations focusing on factors affecting the reliability of Cu/SiLK™ interconnects (IBM), an overview of the Cu/FSG 0.13-μm interconnect process (Intel), and the fabrication of Cu interconnects with porous-SiLK™ (IMEC–Dow Chemical). Researchers from Infineon Technologies and International Sematech presented experimental data for ~45-nm damascene technology, as shown in Figure 2, and reported on the deleterious effect of decreasing line spacing on sheet resistance.

The session on copper metallization covered barriers, copper deposition by supercritical CO_2, copper alloy plating, three-component electroplating chemistry, and the effect of alloying elements on cobalt silicide formation. The session on low-*k* materials addressed the deposition of ultralow-*k* SiCOH dielectric films using plasma-enhanced chemical vapor deposition, the integration of Cu and porous low-*k* materials, and pore-size characterization of mesoporous low-*k* MSSQ films deposited using a macromolecular porogen.

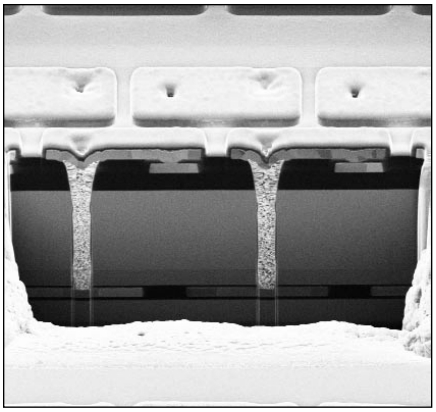

Figure 1. Cross section of a vertically integrated test chip structure, showing 2.5 μm × 2.5 μm interchip vias viewed by focused ion beam.

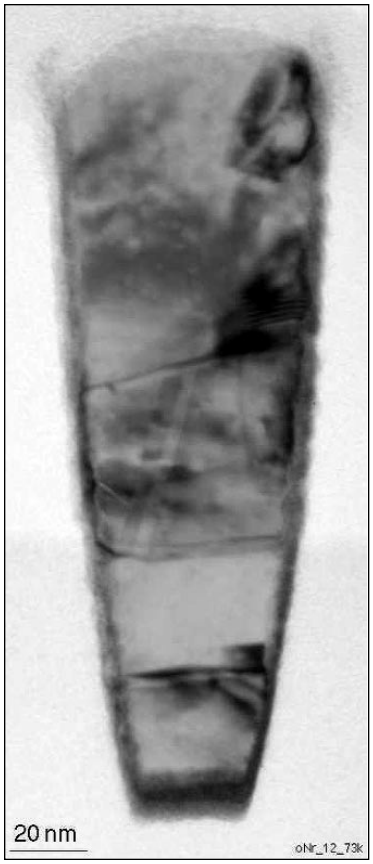

Figure 2. Damascene copper line ~45 nm wide.

R. Joshi (IBM) presented an invited talk on high-performance silicon-on-insulator/Cu static random-access memory and memories in microprocessors in the session on modeling. This session included a discussion on local heating in metallization and on the mechanism of super-conformal Cu deposition. Based on the presentations, the effect of additives on the copper deposition profiles in deep submicron trenches and vias seems to still be an unsolved problem.

D. Edelstein (IBM) compared current barrier systems in the session on barrier layer. He concluded that the TaN/α-Ta is the most suitable technology based on both barrier properties and manufacturing requirements.

The session on reliability featured nine talks, including two on metal-insulator-metal capacitor technologies. The last session of AMC2001 addressed atomic layer deposition (ALD), including an invited paper by K.-E. Ellers (ASML). The oral talks in this session included presentations on TiN ALD, pulsed nucleation of W plug, and ALD of W plug.

Later in the month, AMC convened at a second site, the University of Tokyo in Japan, as ADMETA 2001, chaired by T. Ohba (Fujitsu Research Labs). On October 29–31, ADMETA 2001 attracted ~200 attendees for the regular session and a special tutorial prior to the meeting.

AMC2001 and ADMETA 2001 presented the novel materials and technologies that will be used in future sub-100 nm ultralarge-scale integration technologies. The best barrier technologies and the best material and methods for the application of low-*k* materials is still under debate. Clearly, however, dual damascene technology is scaleable to below 50-nm design rules and advanced vertical integration reached a level that has high synergy with future interconnect technologies.

Papers submitted at both AMC2001 and ADMETA 2001 have been reviewed by the AMC Executive Committee and are scheduled to be published by the Materials Research Society in 2002.

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