## Improved Focused Ion Beam Sample Preparation Techniques for Transmission Electron Microscopy and Failure Analysis of Memristor Devices

Benson Athey<sup>1</sup>, Krishnamurthy Mahalingam<sup>1</sup>, Sabyasachi Ganguli<sup>2</sup>, Albert Hilton<sup>3</sup> and Rohan Dhall<sup>4</sup>

<sup>1</sup>UES, Inc., Dayton,, Ohio, United States, <sup>2</sup>Air Force Research Laboratory, United States, <sup>3</sup>KBR, Beavercreek,, Ohio, United States, <sup>4</sup>Lawrence Berkeley National Laboratory, United States

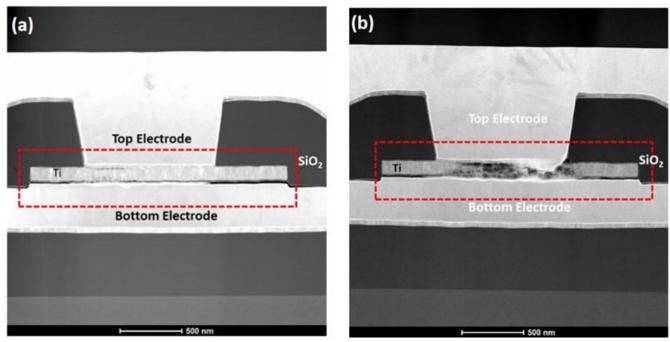
The memristor is a two-terminal device derived from materials that exhibit resistance switching, wherein the resistance of the material is tunable by an applied electric field [1]. This switching process is reversible, and is also non-volatile, so that the change in resistance is maintained for a long period of time even after the applied field is removed. These devices offer distinct advantages over existing flash memory architecture, due to higher switching speed, lower power consumption, better scalability and higher endurance [2]. However, realizing their potential for more advanced applications, as in neuromorphic computing, has been hampered due to device failure associated with variability in current-voltage (I-V) characteristics between individual memristor devices integrated into a single chip. This variability may be attributed to difference in their switching behavior due to factors such as morphology and thickness of individual dielectric layer, and chemistry of the electrode/dielectric interfaces. In this contribution we perform cross-sectional transmission electron microscopy (TEM) to investigate microstructural factors that contribute to device failure. A key aspect in this study is the improvements made to focused ion beam milling (FIB) techniques used for sample preparation, by incorporating procedures used in traditional methods employing Ar+ ion milling.

The memristor device design investigated in this study consisted of a SiO2 dielectric layer sandwiched between Ti-W top electrodes and W bottom electrode. In the present study we present results from two devices: one that exhibited the expected switching behavior and the other, a failed device that exhibited poor resistance values. These devices are labeled normal and shorted device, respectively. The samples were examined by TEM convention bright-field imaging and scanning TEM (STEM) modes. In addition X-ray energy dispersion spectroscopy (XEDS) was also performed to examine the elemental distribution across the electrode/dielectric interfaces. Figures 1 (a) and (b) STEM images of the overall device, wherein the dielectric layer and the electodes have been clearly identified. Figure 2 (a) is the XEDS map of the shorted device where the thin SiO2 layer approximately 20nm thick is clearly delineated between the electrodes. However a more detailed examination of the morphology of this layer indicated significant undulation in the layer thickness. An examination of the XEDS map of the normal sample, shown in Fig. 2 (b) clearly shows significant interdiffusion of Ti into the dielectric layer. While both devices have similar overall structures, it is observed that the difference in electrical properties between the two devices is due to the variability in both morphology and chemical composition of the dielectric layers in the devices examined. Further results on application of the modified FIB sample preparation method for in-situ TEM electrical biasing studies will also be presented.

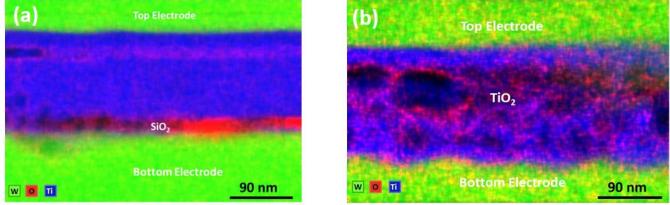
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**Figure 1.** Figure 1 TEM images showing the overall device structure of (a) the shorted device and (b) the normal device



**Figure 2.** Figure 2 XEDS elemental maps of (a) shorted device showing a delineated SiO2 dielectric layer and (b) the normal device showing significant diffuse of Ti into the SiO2 dielectric layer.

## References

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