

HAADF-STEM Investigation of III-V Semiconductors Grown on Nanopatterned Si(001) Substrates

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III-V semiconductors such as GaAs monolithically integrated on Si substrates have a great potential for electronic and photonic device applications [1]. However, the growth of GaAs on Si is very challenging because of defects arising from different crystal structures and the large lattice mismatch of 4 %. One way to reduce the number of defects could be to keep the area of the GaAs/Si interface small.

Here we present ~10, 40, 100 nm in size GaAs nanocrystals (NCs) selectively grown by metal-organic vapor phase epitaxy on top of so called Si(001) nanopillars and nanotips with ~40-80 nm openings embedded in a SiO₂ matrix (Fig. 1a,b). The used nanopatterned Si (001) substrates were fabricated using state-of-the-art 0.13 μm BiCMOS technology [2]. The epitaxial growth of GaAs NCs was optimized and performed at 570°C in a MOVPE AIXTRON 200/4 reactor using AsH₃ and Ga(CH₃)₃ as precursors [3]. Several lamellas were prepared for a STEM investigation of these GaAs/Si nanostructures by a focused ion beam (FEI Helios Nanolab 450S operated at 5-30 kV). High-resolution images were acquired using a HAADF detector in STEM mode on a double spherical aberration-corrected JEOL JEM-ARM200F microscope operated at 200 kV. For electron tomography studies HAADF-STEM tilt series over a -60° to +50° range (with 1° intervals) were recorded around a single rotation axis in a FEI Titan Themis microscope operated at 300 kV with a 10 mrad semiconvergence angle. Alignment and reconstruction were performed using the Inspect3D software. The 3D processing and visualization of the studied heterostructures were done with the Avizo software. The chemical composition of the interfacial area was investigated by energy dispersive X-ray (EDX) mapping using a SuperEDX system equipped with four silicon drift detectors.

In Fig. 2a a high-resolution HAADF-STEM image of a typical ~20 nm GaAs NC grown on top of a Si (001) nanopillar is shown. The detailed examination of the heterointerface reveals the presence a surprisingly large number of 60° perfect misfit dislocations with Burgers vectors $\mathbf{b} = a/2[011]$, $\mathbf{b} = a/2[-10-1]$, and 30° and 90° Shockley partial dislocations with $\mathbf{b} = a/6[121]$, $\mathbf{b} = a/6[211]$, and $\mathbf{b} = a/6[-112]$, respectively. Additionally, other defects such as stair-rod dislocations, stacking faults and grain boundaries were also detected [4]. The same types of defects were observed in the GaAs NCs grown on Si (001) nanotips. An EDX map and tomography results for the GaAs/Si nanopillar are presented in Fig. 2b and c, d, respectively. The presence of a nano-scale corrugated roughness is observed at the interface. In contrast, GaAs NCs grown on nanotips show a concave interface with the Si following the topology of the substrate.

Our results reveal that under identical growth conditions GaAs NCs grown on nanotips are less defective than those grown on nanopillars. This may be due to differences in the three dimensional GaAs/Si interface morphologies as established by electron tomography and EDX measurements. Thus, it is

shown that nanoscale corrugated interfaces are more detrimental to the structural quality of the overgrown GaAs nanocrystals than surface steps (resulting in concave GaAs/Si interfaces) [5].

References:

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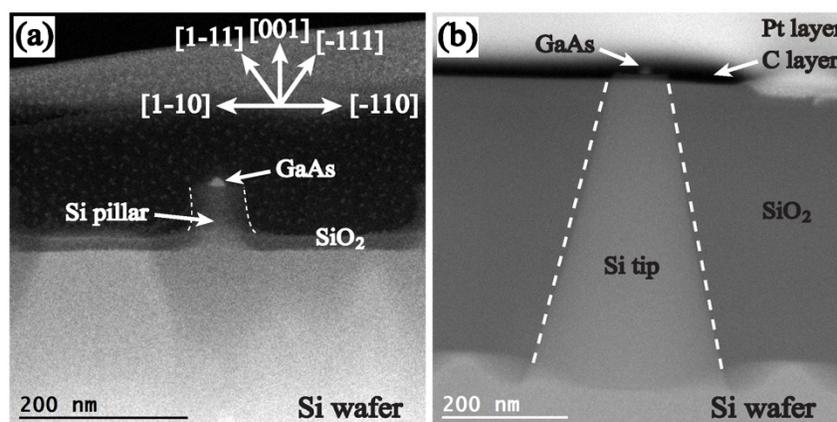


Figure 1. (a), (b) Cross-sectional HAADF-STEM images of GaAs NCs with ~ 15 - 20 nm in size grown on top of a Si(001) nanopillar and nanotip with ~ 40 - 80 nm openings embedded in a SiO_2 matrix, respectively.

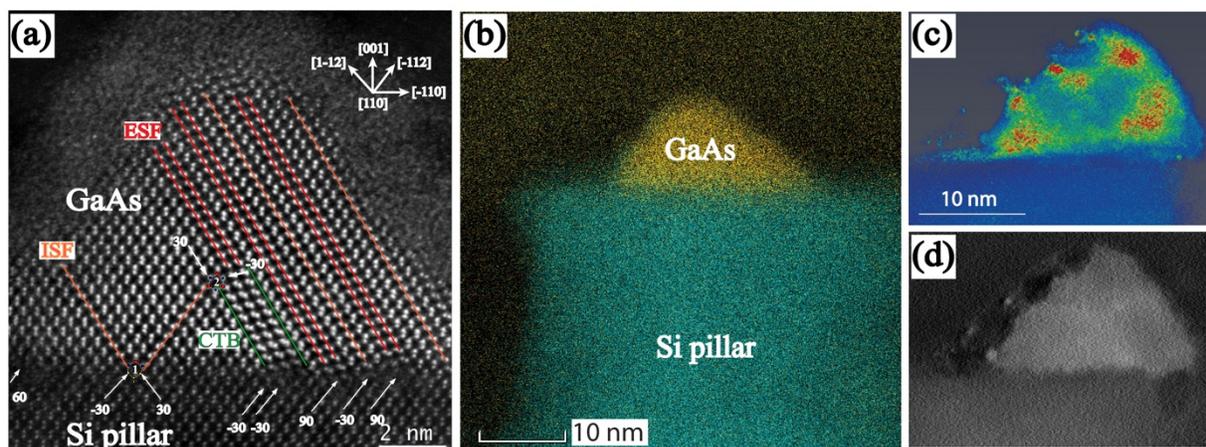


Figure 2. (a) High-resolution HAADF-STEM image of a GaAs NC grown on top of a Si(001) nanopillar. White arrows indicate the positions of the dislocations. Intrinsic and extrinsic stacking faults, with single and double lines, respectively, are marked in red, coherent twin boundaries – in green. (b) EDX map and (c, d) tomography results (volume-rendered 3D reconstruction and xy-orthoslice, respectively) showing the nano-scale wave-shaped roughness at the GaAs/Si interface.