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A TEM Nanoanalytic Investigation of Pd/Ge Ohmic Contacts for the Miniaturization and Optimization of InGaAs nMOSFET Devices.

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In this paper, a nanoanalytical investigation of electron beam evaporated PdGe ohmic contacts to an n^+ $In_{0.53}Ga_{0.47}As$ layer using electron energy loss spectroscopy (EELS) is presented. The chemical information reported in this paper has been obtained using EELS spectrum images (SI) that allow increased spatial resolution which is essential in inhomogeneous systems.

As the size of III-V devices decreases, ohmic contacts and their performance become increasingly important. In addition to low resistance, these contacts need to show thermal stability as well as lateral and depth uniformity. AuGeNi ohmic contacts have been widely used as they show relatively low specific contact resistivity. However, as reported in [1], they have the drawback of poor uniformity due to the Au diffusion into the III-V substrate. Obviously this strongly limits them for scaling purposes. In addition, with the quest for co-integration of III-V and silicon MOSFETs for ultimate CMOS applications, silicon compatible III-V device process modules, which are gold-free, are required. PdGe based ohmic contacts have demonstrated as low resistance as AuGeNi solutions with better uniformity along the interface with the III-V substrate [1]. These contacts are formed by depositing a layer of Pd on the III-V followed by a thicker one of Ge. During the annealing process, the Ge reacts with the Pd forming PdGe. However if the annealing process is carried out at high temperature (>300°C), the Ge will also react with the III-V substrate. The behaviour of this type of contact will be affected by the nature of the species present at the interface and the actual roughness along the interface [2]. Therefore a detailed chemical analysis across the contact region is important in optimizing the deposition and annealing conditions. The contacts of this study are capped with Ti/Pt that acts as a barrier to upwards Ge diffusion during the annealing process [3].

The 70 nm Pd, 100 nm Ge, 30 nm Ti and 40 nm Pt ohmic contact stack was deposited by electron beam evaporation onto a 500 nm thick $In_{0.53}Ga_{0.47}As$ layer silicon doped to $1x10^{19}$ cm^{-3}, grown on a semi-insulating InP substrate. The sample was then cleaved and one half went through a rapid thermal annealed for 10 seconds at 400 ^{o}C. TEM specimens of both the unannealed and annealed samples were prepared by standard cross-sectioning; all the images obtained and chemical analysis undertaken were carried out using a FEI Tecnai F20. The experimental conditions employed during the EELS analysis were: probe size, α/2, β/2 respectively 0.75nm, 9mrad and 22mrad. The unannealed sample does not show, at a large scale, any sign of major reactions between the ohmic contact and the substrate across the whole contact region as shown in Fig. 1. Ge and Pd layers appear to be amorphous although some lattice fringes can be observed at ~10nm in the substrate when the image is taken at higher magnification. Fig. 2 shows a low magnification image of the annealed sample. Most of the Ge has reacted with all the Pd forming a PdGe granular structure that extends to the III-V substrate. The interface is now fairly rough and it is also quite difficult to distinguish where the original interface was before the annealing. However, some of the Ge next to

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the Ti barrier layer has not reacted as shown in Fig. 2. Fig. 3 is a high-resolution TEM image of the contact/substrate interface taken from the annealed sample. It confirms that most of the contact region next to the interface has crystallized with the same orientation as the InGaAs substrate. For the annealed sample, the EELS line spectrum images were taken across the selected region shown in Fig. 4, using 1.9nm step size. Fig. 5 shows the In, Ga, Ge, As, Pd edge intensities extracted from that region. Ge has either directly penetrated the Pd layer or propagated along grain boundaries and diffused into the InGaAs more strongly than the Pd; most probably resulting in locally n+ doping the InGaAs along the interface region. Ga and In have diffused into the contact region with Ga propagating further. The interface region extends for ~12nm between the PdGe contact and the substrate. In the InGaAs region, a 2nm layer rich in In and deficient in Ga has been detected. This is also shown in Fig. 4 as bright layer. The As profile does not vary significantly, suggesting the presence of InAs, whose formation mechanisms are the subject of current investigation.

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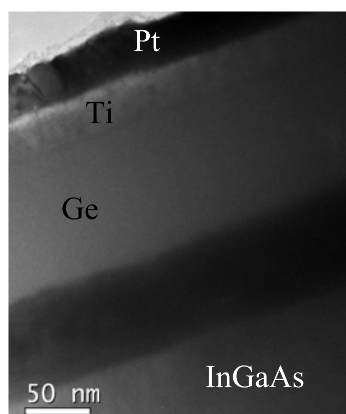

Fig. 1 TEM micrograph of the ohmic contact stack in the unannealed sample.

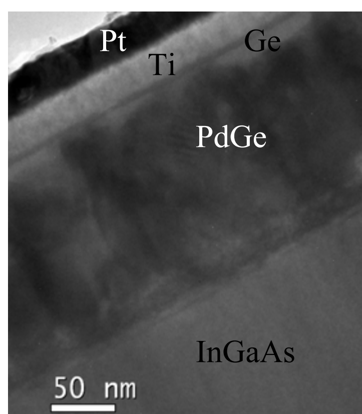

Fig. 2 TEM micrograph of the ohmic contact stack in the annealed sample.

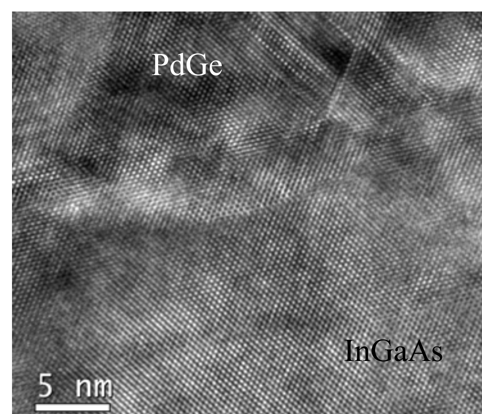

Fig. 3 High-resolution TEM image of the interface region in the annealed sample.

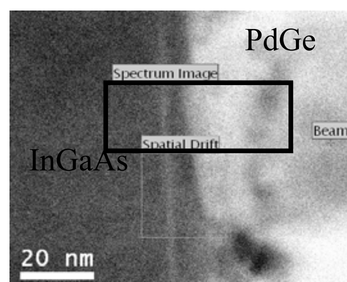

Fig. 4 ADF STEM survey image of the annealed sample. The black box is the area used for the acquisition of the EELS SI. The bright layer is the In rich layer as shown in Fig. 5.

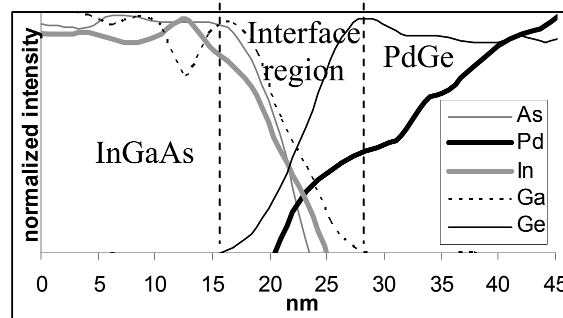

Fig. 5 As, Pd, In, Ga and Ge edge intensity profiles extracted from the region in the black box of Fig. 4.

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