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Local Stress Measurements in Microelectronic Devices Using HREBSD

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Because of the elevated temperatures required for the manufacture of microelectronic devices, significant stresses develop due to differences in coefficient of thermal expansion between different layers. These stresses are significant drivers of failure, including cracking, delamination and void nucleation. The most common techniques for determining local stresses in microelectronics are curvature measurements and finite element elasticity models. Bulk curvature measurements lack the resolution to determine stresses around complex features, and finite element techniques are limited by the need to model the precise geometry of the part, as well as the need to model more complex relaxation phenomena. Measuring the local stress development around failure initiation sites to develop better failure models is impossible with both of these techniques. In this study local stresses are measured using high resolution electron backscatter diffraction (HREBSD).

HREBSD is a scanning electron microscope-based diffraction technique where patterns are collected with camera, and then image correlation is applied to the diffraction patterns to determine relative elastic strains and misorientations between patterns [1]. This technique is much more accurate than conventional EBSD, but still has its limitations. The primary limitation it has is that it is a surface technique. Layers of interest in microelectronics are often embedded in other layers, the removal of which would release most of the stress on the layers of interest. To circumvent this issue, two separate sample preparation techniques are explored: back-thinning of the substrate, and cross-sectioning. With back-thinning, HREBSD was not conducted on the metallic layer of interest, instead distortions in the thinned substrate were measured. This localized information could then be related to the stress in the metallic layer to stresses around voids in the metallic layer using finite element analysis. Cross-sectioning is a more straight-forward approach to this problem because it exposes the relevant layers directly. However, it comes with the downside of relieving more of the stress and must be similarly augmented with analysis. An example of the distortions measured in the substrate of a microelectronic device where the effects of individual conduction lines are discernable is shown in Figure 1 [2].

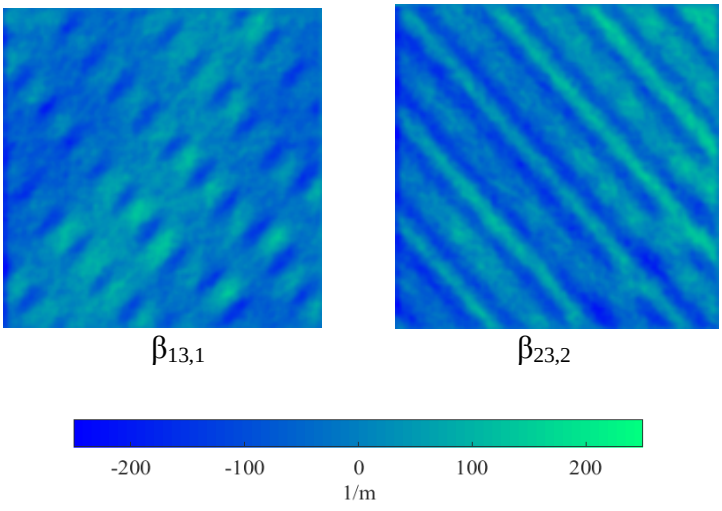

Figure 1. Selected distortion derivatives calculated with HREBSD from the thinned substrate of a microelectronic device. Note that the effect of individual conducting lines and vias is visible. The area shown is 150 microns square.

References:

[1] Ruggles, T. et al., Ultramicroscopy **195** (2018), p. 85.
[2] This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525.

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