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Challenges and Opportunities in Characterizing Modern Nano-Devices

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In the past 40 years, transistor scaling has been following Moore's Law, the number of transistors on a chip doubles about every two years. Cost efficiency, performance enhancement and energy efficiency are the driving forces behind the continuous scale down. Nano-scale feature sizes in current technology keep raising greater challenges to both structural and chemical characterization of semiconductor devices. TEM with its unique atomic resolution and analytical capabilities becomes crucial and irreplaceable in supporting technology research and development as well as product manufacturing in semiconductor industry.

To improve transistor performance and reduce power consumption, electric oxide thickness (Tox) is getting thinner together with shrinking transistor dimensions. Electric fields within the gate oxide grow larger and gate oxide reliability becomes an issue. Figure 1 shows an example of dielectric breakdown induced epitaxy (DBIE) in a typical polycrystalline Si gate device. The unit was stressed to fail and then fault isolated. The lattice planes across the gate oxide matches the underlying Si substrate indicating Si re-growth from the channel. Another dielectric breakdown example is illustrated in figure 2, where simultaneous EDX and EELS spectroscopic imaging of the breakdown area was collected on probe aberration corrected microscope. The top image in (c) shows STEM HAADF intensities at the scanned area. The middle and bottom maps in (c) were spectroscopic images extracted from EDX Si-K peak and EELS O-K edge, respectively. EELS spectra of Si-L edge at the marked spots are shown in (d). Spots 1 and 3 are at normal Si substrate and gate oxide areas, thus exhibiting normal Si-L_{23} edge features for crystalline silicon and silicon dioxide, whereas spot 4 at broken-down gate oxide area shows combination of the two indicating O depletion and Si re-growth as a result of the dielectric breakdown.

As traditional SiO_2 gate oxide scaling reaches a bottleneck due to molecular requirements, new materials – high-k gate dielectric bundled with metal gate – has been successfully implemented by Intel into 45nm [1] and 32nm [2] processes to reduce gate leakage and enable continuing Tox scaling. Other novel materials and technology, such as III-V based quantum well field effect transistor [3], tri-gate transistor [4], semiconductor nanowires, are in study for future high-speed and low-power transistors digital circuit applications. In addition to atomic scale imaging and analytical capabilities, various special TEM techniques and novel sample preparation methods will be discussed, such as nano-diffraction to determine localized strain and STEM tomography to identify small defects, among others. As process development and device scaling continues some of these novel methods may become routinely applied in order to continue the expected solution pace.

References

[1] K. Mistry et al, *IEDM Tech. Dig.* December (2007) 247-250.
[2] P. Packan et al. IEDM 2009
[3] M. K. Hudait et al. IEDM 2007
[4] J. Kavalieros et al. VLSI 2006
[5] ORTEM lab artists are gratefully acknowledged for their fine TEM sample preparation skills.

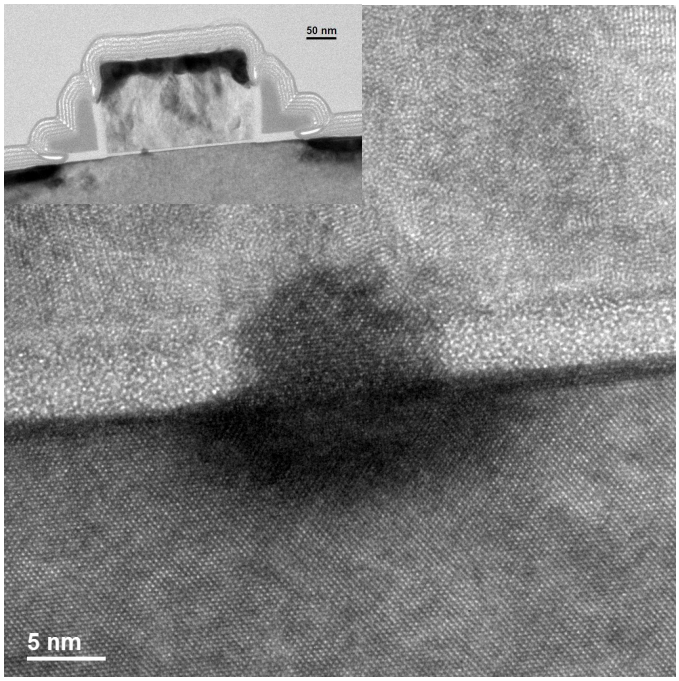

FIG. 1. HRTEM image of an example of strain-induced epitaxy across SiO_2 gate dielectric. The inset at top left corner shows the complete gate with source and drain silicide.

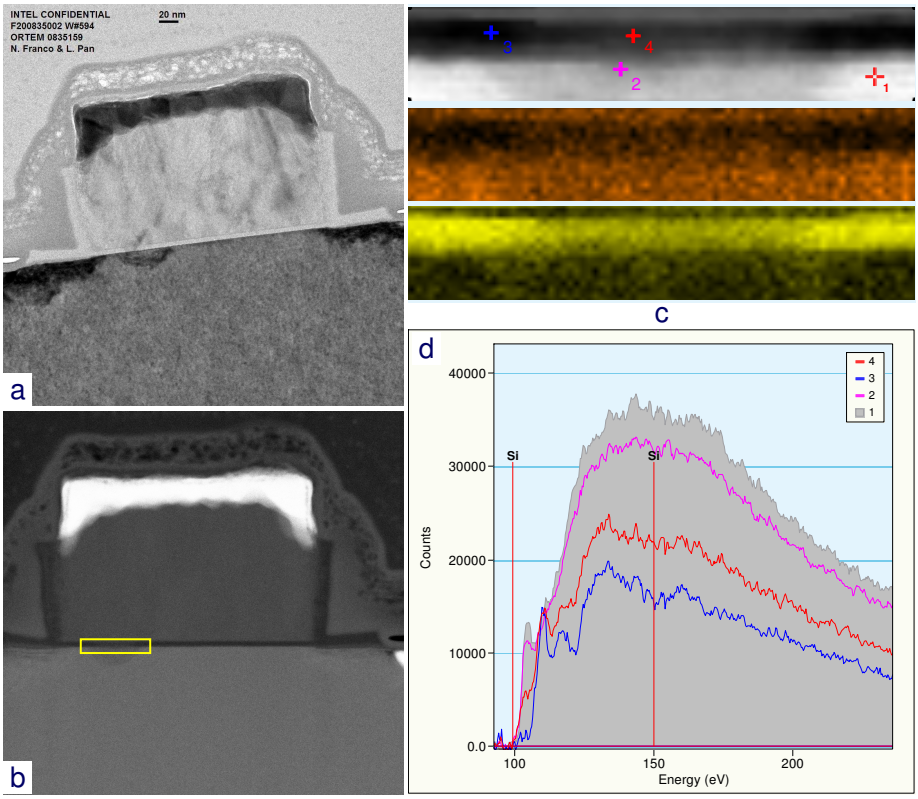

FIG. 2. (a) BF TEM and (b) DF STEM images of a failed gate, (c) spectroscopic images of the scanned rectangular boxed area in (b), top one is the STEM HAADF intensity map, middle one is Si-K peak EDX map, bottom one is O-K edge EELS map, (d) EELS spectra of Si-L edge at the spots marked in (c).

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