A repetitive 800 kA linear transformer drivers stage for Z-pinch driven fusion-fission hybrid reactor

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Abstract

This paper presents the design and tests of a repetitive 800 kA fast linear transformer driver (LTD) stage aimed for the Z-pinch driven fusion-fission hybrid reactor (Z-FFR). The LTD stage consists of 34 parallel basic resistor R, inductor L, and capacitor C (RLC) circuits each made up of two 100 kV/40 nF capacitors, a multi-stage gas switch and Metglas magnetic cores. The stage can deliver about 800 kA current pulse with rise time of 100 ns into the matched liquid resistive load at a repetitive frequency 0.1 Hz. A novel method to trigger the stage via a continuous internal trigger bus composed by a single cable has been proposed and demonstrated. The experimental results show that the new trigger method is feasible and reliable. A 140 kV, 25 ns rising time trigger pulse, and a 5.2 kA, 30 µs width pre-magnetization current pulse which can operate at a repetition rate 0.1 Hz were used in this stage to insure the LTD stage generating a 80 kV/800 kA current pulse every 10 s. A multi-stage gas switch that has a lifetime in excess of 10,000 shots and a jitter less than 3 ns one sigma agrees well with the demand of Z-FFR. The electrical behavior of the stage can be predicted from a simple RLC circuit, which can simplify the design of various LTD-based accelerators.

Keywords: Current pulse; Gas switch; Linear transformer driver; Novel trigger method; Repetition rate

1. INTRODUCTION

Z-Pinch driven fusion-fission hybrid reactor (Z-FFR) proposed by the research team of China Academy of Engineering Physics can be used for production of electricity with the advantages of safety, economy, permanence, and environment friendliness(Peng, 2010; Peng & Wang, 2014). The design fusion yield is 1.5 GJ per pulse with 6 pulses per minute. The energy gain of the fission blanket is more than 20 and the nuclear power of the Z-FFR is about 3000 megawatts. The Z-FFR concept uses a linear transformer driver (LTD) accelerator which can deliver tens of mega-ampere pulse current with width of 100 ns to a wire array Z-pinch load with repetitive frequency of 0.1 Hz, and a recyclable transmission line to connect the LTD driver to a high-yield fusion target inside a thick-liquid-wall power plant chamber.

LTD that was first conceived and developed at High Electronic Institute in Tomsk is a new pulsed power architecture that may dramatically reduce the cost and size of future

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pulsed-power accelerators (Kim et al., 2001; 2004). At Sandia National Laboratories, a 500 kA LTD cavity have been fired up to now, approximately 13,000 shots at repetition rate higher than 5 shots per minute without switch or capacitor failure (Mazarakis et al., 2007). In LTD, DC charged capacitors are discharged in parallel to provide a 100 ns wide power pulse to a load directly without any of the pulse compression hardware used in traditional pulsed-power accelerators. The biggest advantage of the LTD drivers is the possibility of a repetition rated operation. According to the capacitor specifications and switch pressurization and fast purging, LTD can reliably generate sequential current pulses with repetition rate 0.1 Hz which make LTD drivers to be an optimal choice for inertial fusion energy where the required repetition rate is estimated to be the same range (Mazarakis & Olson, 2006; Mazarakis et al., 2006; Olson et al., 2007; Deng et al., 2014).

The basic unit of a LTD stage which is called a "brick" typically consists of two capacitors, a triggered gas switch, annular magnetic core, and a load which may be magnetically insulated transmission line (MITL) in vacuum, liquid resistive load or de-ionized water transmission line (Kim *et al.*,

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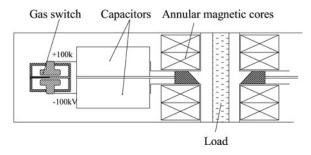


Fig. 1. Schematic of a basic LTD brick.

2009; LeChien *et al.*, 2009; Woodworth *et al.*, 2011). Figure 1 shows a typical LTD brick. Two capacitors are charged to opposite polarities with a gas switch between their high-voltage outputs. When the switch is triggered and conducts current, a voltage pulse is induced on the opposite ends of the capacitors. This voltage pulse attempts to drive current around a loop formed by the metallic case of the LTD brick. The annular magnetic cores, however, block current from flowing in this loop until the magnetic cores saturate. This results in a large, fast-rising voltage pulse been impressed on the load in the center of the stage. Losses in the annular magnetic cores can reduce the peak power on the load by 10–20% depending on the detail configurations of the system.

Normally, multiple bricks are stacked in parallel around a central load to form a LTD stage which can deliver more than 1 MA pulse current to the load with 100 ns width. Multiple stages can be stacked in series and in parallel, to generate higher voltage and higher current pulse into the load (Leckbee *et al.*, 2006; 2008; 2011; Stygar *et al.*, 2007; Savage *et al.*, 2011).

In Section 2 of this paper we describe the design of the 0.1 Hz, 800 kA, and 100 ns fast LTD stage developed at Institute of Nuclear Physics and Chemistry (INPC), China. In Section 3 we present tests of the LTD stage with liquid resistive load. The supporting systems such as control system, pre-magnetization system, triggering system, and novel trigger way will be described too. In addition, the electrical performance and experimental results of the LTD stage are discussed and explained in detail.

2. DESIGN OF FAST 0.1 HZ 800 KA LTD STAGE

The design of the 0.1 Hz 800 kA LTD stage is shown in Figure 2. The outside diameter of the stage is 2560 mm, the length along the main axis is 214 mm. Inside the stage is located the capacitor bank with the switches, charge and trigger air-core inductance, and the Metglas magnetic cores. The capacitor bank is made up of 68 storage capacitors that are arranged as 34 pairs. The capacitors in each pair are charged in opposite polarity up to ± 100 kV and switched into the load by closing the multispark gap switch. The China XIMAI double ended capacitor (40 nF, 100 kV, and 30 nH) used in the stage is compact with length of 18.2 cm, width of 16 cm, and thickness of 7 cm. The four-spark gaps switch developed at Northwest Institute



Fig. 2. Design of 0.1 Hz LTD stage with a liquid resistor load. (a) Side section view of the stage. (b) Overview of the stage.

of Nuclear Technology (NINT) has been used in our stage (Liang *et al.*, 2006; Liu *et al.*, 2009). The switches shown in Figure 3 are relatively small with diameter of 9.4 cm and height of 12.5 cm. They have four 7 mm gaps. The DC voltage is distributed between four switch gaps with a corona discharge. The switches can operate reliably with dry air at a pressure of 300 kPa for ± 100 kV charging voltage triggered by 140 kV, 25 ns rising time pulses.

In the stage the 1.65 m outer diameter Metglas magnetic core had four separate rings, each ring being wound with a 25 µm thick, 30 mm wide 2605SA1 Fe-based amorphous tape sandwiched in a 1 µm thick SiO₂ coat insulation. The rings are molded into a glass fiber compound to stabilize the turns and isolate the rings from each other. The glass fiber encapsulation of each ring has a size of 1.65 m outer diameter, 1.4 m inner diameter, and 30 mm height. The magnetic induction at saturation of 2605SA1 is $B_S = 1.5$ T at H = 80 A/m, the residual induction is $B_R = 1.2$ T. The total cross-section of the Metglas core of four rings is 73 cm². The volt-second integral of the entire core is $VS_C^P = 19.7 \text{ mVs}$ with passive premagnetizing ($\Delta B = 2.7 \text{ T}$). In $\pm 100 \text{ kV}$ shots, the total volt-second product impressed across the magnetic cores may be 15 mVs estimated by square pulse with 150 ns width, well below the 19.7 mVs product of the Metglas cores.

The set of two capacitors, the switch, and the buses connecting the capacitors from one side with the switch and from the opposite side with the azimuthally gap is called brick and represents the basic element of the stage. All the 34 bricks in the stage are connected in parallel and located evenly in a circular array around the axis.

In order to achieve a fast rise time output pulse, the inductance of the brick must be kept as low as possible. An estimated inductance of the brick is about 270 nH which is the sum of the two capacitor inductances (60 nH), the switch inductance (120 nH), and the inductance of the circuit bushes (90 nH). Then according to the formula of a simple resistor-inductor-capacitor (RLC) circuit, $t_{\rm rise} = 1.21({\rm LC})^{0.5}$ and $R_{\rm matched} = ({\rm L/C})^{0.5}$ (Mazarakis & Olson, 2006; Mazarakis *et al.*, 2009), the rising time and matched load of the stage is, respectively, \sim 89 ns and \sim 0.11 Ω .

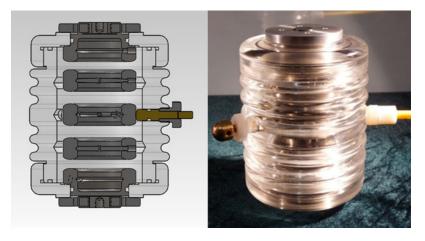


Fig. 3. Four-spark gaps switch developed by NINT, China.

The inductance of each charging isolated inductor is 6 μH and the inductance of each trigger isolated inductor is 4 μH . A novel method to trigger the stage via a continuous internal trigger bus composed by a single cable has been developed. The trigger pulse for the stage was generated by discharging two 20 nF capacitors to the same voltage to the brick in parallel by closing a four-gap switch. The trigger pulse reaches the 34 switches synchronously via a transmission line.

3. TESTS OF FAST 0.1 HZ 800 KA LTD STAGE

3.1. Experimental Results of the LTD Stage

In the tests of the stage, 36 liquid resistors are connected as load in parallel and located in a circular array around the axis. The LTD stage with all the components except the top flange removed was shown in Figure 4. The stage was filled with transformer oil during operation. The oil was filled and drained through filters that removed particles and moisture. It is important and beneficial for high voltage insulation to draw off all air bubbles in the stage. During normal operation, the top capacitors are charged to positive voltage and the bottom capacitors are charged to negative voltage.

In order to operate at 0.1 Hz, we developed the supporting systems such as capacitor charging, switch pressurization,

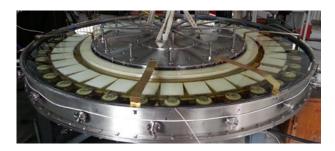


Fig. 4. 0.1 Hz, 800 kA, and 100 ns LTD stage with the top flange removed. The 34 switches, charging and trigger isolated inductors, Metglas magnetic cores, and the top capacitors are also shown. 36 liquid resistive loads in parallel are concealed in the center of the LTD stage.

switch vacuum purging, pre-magnetization, and triggering system. All of these have exceeded the 0.1 Hz repetition rate and automated controlled by a computer via optical fiber communication. All the supporting systems operate one shot with the sequence described below within 10 s, shown in Figure 5. In the first 5 s period, pre-magnetization system will be charged by a $\pm 50 \, \text{kV} / 10 \, \text{mA}$ constant current power supply; switches in stage and trigger generator will be purged and pressurized; at the fifth second the premagnetization system generates a 5 kA/30 µs current pulse shown in Figure 6 to set the magnetic cores. The following 5 s period, switches in pre-magnetization system will be purged and pressurized; and the same period all the capacitors in stage and trigger brick will be charged to $\pm 80 \text{ kV}$ separately by a $\pm 100 \text{ kV}/50 \text{ mA}$ constant current power supply; at the tenth second the trigger system generates a 140 kV, 25 ns rising time pulse to trigger all the 34 switches in the stage synchronously. Then the stage generates about 800 kA, 100 ns rising time current pulse shown in Figure 7 into a matched load. If conditions are normal, the sequence repeats every 10 s.

3.2. Four-spark Gap Switch

Figure 8 shows a schematic of a brick of the LTD stage using the four-spark gap switch. Two 100 kV/40 nF capacitors are

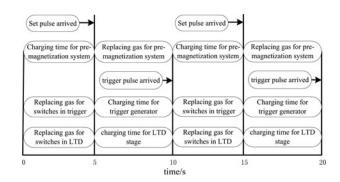


Fig. 5. Time sequence control of the LTD stage.

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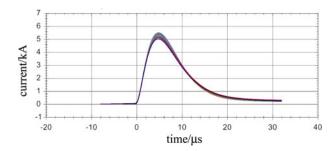


Fig. 6. 24 shots sequential output pulse currents to set the magnetic cores with the repetition rate 0.1 Hz. The liquid resistive load in series was used as a damper in the circuit of the pre-magnetization system. And along with operating with repetition rate 0.1 Hz, the value of water resistance will gradually diminish because of the rising temperature. Then the peak pulse current into the liquid resistive load will gradually increase.

connected with a four gaps switch and the other ends of the capacitors are connected simply to each other through a matched liquid resistive load. A Rogowski coil is placed between the load and ground to monitor the current in the circuit. A resistive divider monitors voltage across the resistive loads to allow us to verify that the value of the resistive loads has not shifted.

The capacitors are charged to $\pm 80\,\mathrm{kV}$, 80% of the full voltage. A positive electrical trigger was applied to the midplane of the switch. The trigger pulse was a nominal 140 kV pulse with a 25 ns rising time. The switch-testing apparatus can operate at repetition rate 0.1 Hz automatically controlled by a computer. The switch can operate very well with 200 kPa dry air. The delay, jitter, lifetime, and the inductance of the switch were also tested. The switch was fired more than 10,000 shots with a repetition rate of 6 shots per minute without failure. The trigger delay time and jitter (one sigma) are about 40 and 2.5 ns, respectively.

Figure 9 shows a typical pulse current waveform. The brick inductance, including the switch inductance, can also be estimated according to the output current waveform. The period of the pulse current is about 464 ns. Then the total inductance of the brick can be calculated to be 272.7 μ H that agree well with the estimated value in Section 2.

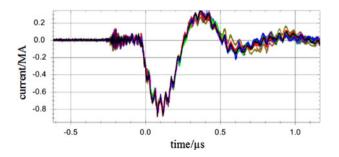


Fig. 7. 24 shots sequential output pulse currents of the LTD stage into near matched load with the repetition rate 0.1 Hz. The capacitors of each brick were charged to $\pm 80 \, \text{kV}$ and the liquid resistive load is about 0.1 Ω ; the peak pulse current is about 800 kA and peak power into the load is about 64 GW.

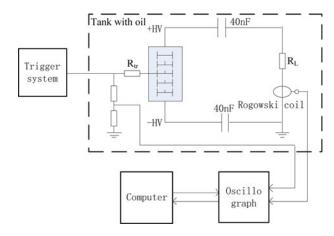


Fig. 8. The schematic of testing the four-spark gap switch using a brick of LTD stage.

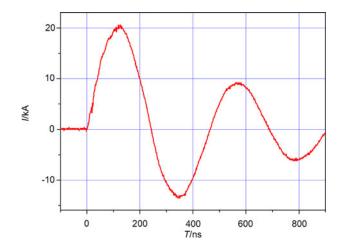


Fig. 9. Typical waveform of the output current of the brick with about 3 Ω liquid resistive load.

3.3. Novel Trigger Method

Normally a trigger cable can deliver a trigger pulse to trigger six to eight switches of the LTD stage (LeChien *et al.*, 2009; Zhou *et al.*, 2010). So it may need at least four trigger cables to fire the LTD stage which contains 34 bricks. In order to simplify the trigger system, a novel method to trigger the stage via a continuous internal trigger bus composed by a single cable has been developed. The trigger brick is charged to the same voltage as the stage, and it comprises 2, 100 kV, 20 nF capacitors and a, 200 kV, air filled switch (similar to the stage switches, except triggered differently).

Figure 10 shows the sketch of novel trigger method. The trigger pulse generated by trigger brick is firstly divided into two and reached the point A and B via a quarter angle transmission line. And then it is divided into four and arrived the point C, D, E, and F of the trigger bus simultaneously by transmitting another eighth circle distance. The overview of the trigger pulse transferring net is shown in Figure 11. The red line is the angle transmission line, and the outer metal

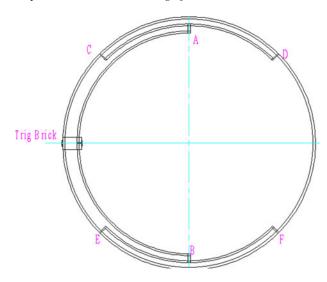


Fig. 10. Sketch of a novel trigger method.

ring is the trigger bus. In the tests, two trigger ways using one trigger cable and four trigger cables to trigger the LTD stage separately are compared. The results show that using one trigger cable to trigger the LTD stage is as reliable and efficient as using four trigger cables. It is very inspiring and important to simplify the trigger system of future high current petawatt-class *z*-pinch accelerators (Stygar *et al.*, 2007).

3.4. Parameters of the LTD and Discussion

In the tests, the synchronizer DG535 generates a 5 V Transistor-Transistor Logic (TTL) synchronous pulse to start the trigger system of the LTD stage. The trigger system produces a 140 kV, 25 ns rising time pulse after 1.34 μ s to trigger the LTD stage with jitter time 21 ns. Then the LTD stage generates an 800 kA, 100 ns rising time, 100 ns width current pulse into the near matched load with delay time 190 ns. Figure 12 shows the waveform of shot 2555. The period of the pulse current is 565 ns. The equivalent capacitance of the stage is 680 nF. Then the equivalent inductance of the stage is 11.9 nH calculated by formula $T = 2\pi(LC)^{0.5}$

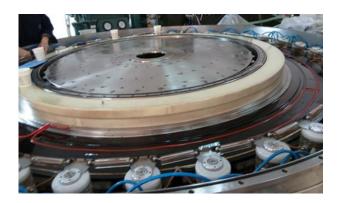


Fig. 11. Overview of the trigger pulse transferring net.

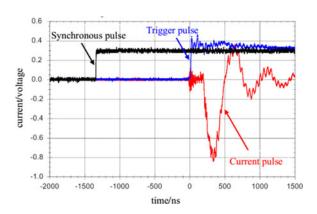


Fig. 12. The LTD stage output waveform of shot 2555. The capacitors of each brick were charged to $\pm 80 \text{ kV}$ and the liquid resistive load is about 0.1.0

which is higher than the value 8 nH estimated by 34 bricks in parallel. So the inductance of load area which has a big contribution to equivalent inductance of the LTD stage is about 3.9 nH. So decreasing the inductance of the power transmission and load area is beneficial to increase the peak current of the LTD stage. In fact, considering the inductance of the load area the matched load should be 0.13 Ω higher than the 0.1 Ω in tests. Therefore the LTD stage can deliver about 840 kA current pulse into a matched load in $\pm 100~\rm kV$ shot.

4. CONCLUSION

In the present work the fast 800 kA LTD stage built with 34 separate bricks has been developed and tested in INPC, China. The power pulse delivered to a near matched load 0.1 Ω has a peak value of 64 GW and a rising time of 100 ns. The 800 kA LTD stage was tested with resistive load. A novel trigger way in which only one trigger cable triggers the stage has been proposed and demonstrated the same reliability and efficiency as using four trigger cables. The experimental results are in excellent agreement with numerical simulations. The LTD stage with brick inductance 272 nH and load inductance 3.9 nH can deliver an 840 kA, 100 ns rising time, and 100 ns width pulse current into a matched load 0.13Ω with a repetition rate 0.1 Hz. Up to now the stage has been fired approximately 10,000 shots and more than 4000 shots are fired at repetition rate, 6 shots per minute. Tests with vacuum self-MITL are undergoing, and further results will be presented in future paper.

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