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High Frequency AlGaN/GaN MODFET's

L. Eastman, K. Chu, W. Schaff, M. Murphy, N. G. Weimann
Dept. Electrical Engineering, Cornell University

T. Eustis
Dept. Material Science, Cornell University

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Abstract

Short-gate MODFET's of AlGaN/GaN on Sapphire have been fabricated and characterized with gate lengths in the .12 - .25 µm range. Values of f_t = 50 GHz and f_{max} = 100 GHz have been obtained. Analyzing the performance, the average electron transit velocity is shown to be 1.25 x 10^7 cm/s and in some cases well under that value. This compares with theoretical predictions of ~ 2.0 x 10^7 cm/s. The electron scattering effects of dislocations, which are charged, are modeled to explain the lower mobility. Ion bombardment or dry etching is used for mesa isolation. Ti/Al/Ti/Au sintered for 100 seconds at 800 °C is used to yield ohmic contacts of .5 - 1.0 Ω-mm. Pt/Au Schottky gates are used. A high breakdown voltage, exceeding 100 V even for short gate MODFET's, shows that ten times higher load resistance values are possible, compared with GaAs MODFET's. Normalized output power levels well over 10 W/ mm are thus projected for GaN MODFET's on SiC substrates, where the thermal conductivity is about 5W/cm-°C. with future integrated traveling-wave, power-combining circuits, output power > 100 W at 10 GHz is predicted.

1. Introduction

MODFET's based on GaN on SiC substrates will be able to amplify microwave signals up to power levels above 100 W at 10 GHz. This is due to the high GaN breakdown field (~4 MV/cm), and the high thermal conductivity (~5 W/cm-°K) of the SiC substrate. Channel current exceeding 500 mA/mm is possible [1] in addition to breakdown voltages exceeding 100 V [2]. It is then possible to have both high power per millimeter of periphery, as well as a high load resistance for a millimeter periphery. Together, this allows larger periphery as well, thus yielding very high total power.

1.1. Electron transport in GaN MODFET's

The low field mobility of electrons in bulk Wurtzite GaN is limited by charged states that are dislocation-related, as well as by isolated donor ions and phonons. With no dislocations or donor ions, the 300°K phonon-limited mobility is near 2,000 cm^2/V-s. An equilibrium model has been developed for the charged dislocation-related states, centered about 2.15 eV below the conduction band, and the corresponding depletion nearby. The combined scattering effects reduce the mobility for both highly-doped and lightly-doped material, for a given dislocation density. The dislocation density depends on the nucleation methods used at growth initiation, usually ranging from 3 x $10^9/cm^2$ - 3 x $10^{10}/cm^2$. The total mobility expected from this model, as a function of carrier density as depleted by the charged dislocation-related states, with the dislocation density as a parameter, is shown in Figure 1. Data from Prof. Moustakas are shown for two different nucleation methods, where two different dislocation densities would result.

When a two-dimensional electron gas (2DEG) is formed in a thin GaN quantum well with AlGaN barriers, the Fermi level for the 2DEG is .1 - .2 eV above the ground state. This raises the mobility of the electrons due to reduced scattering from any charges, in proportion to the Fermi level. As a result, values of 2DEG mobility from 400-1,600 cm^2/V-s have been achieved, even with the present values of dislocation density. The mobility is expected to be highest for quantum wells that are < 100Å thick, so that only ground state electrons are present. 2DEG density values are usually higher than expected from the design, possibly due to piezoelectric effects.

The average drift velocity at high fields in bulk GaN, or in GaN MODFET's, is expected to be above 2×10^7 cm/s [3]. These high fields extend increasingly toward the drain with higher applied drain-source voltage. Based on the intrinsic f_t value derived from the data below, the average transit velocity is $\geq 1.25 \times 10^7$ cm/s when only the effective gate length is considered - without the extended high-field region. This result is consistent with an average drift velocity of ~ 2×10^7 cm/s over an extended region.

2. Fabrication

Heterostructure Field Effect Transistors (HFET's) were fabricated on an OMVPE grown wafer. The layer structure included, from the sapphire substrate, a 1-µm undoped GaN buffer, a 1000-Å n-doped channel, a 30-Å undoped AlGaN spacer and a 300-Å n-doped AlGaN barrier layer (Figure 2) [4]. All AlGaN layers had an aluminum mole fraction of 15%. The HFET's were fabricated through ohmic metallization, implant isolation and gate metallization. The ohmic metals used were Ti annealed at 800°C for 120 s and unannealed Ti/Au [1]. Proton implantation was used for isolation, after which Pt/Au gate metals were deposited using electron-beam lithography and lift-off.

3. Measurements

DC measurements on the HFET's showed a transconductance of 120 mS/mm and a peak drain current of 550 mA/mm for the devices with annealed Ti ohmics, while the Ti/Au devices demonstrated 80 mS/mm and 450 mA/mm (Figure 3). The difference in DC performance was a direct consequence of the difference in ohmic contact resistance. TLM measurements gave a contact resistance of 4.8 Ω-mm for the annealed Ti contacts and 10 Ω-mm for the unannealed Ti/Au contacts. The higher contact resistance of the Ti/Au devices slightly deteriorated their DC performance.

RF measurements were also performed on the HFET's. S-parameters were measured up to 26.5 GHz, and f_t and f_{max} were determined from 6-dB-per-octave drop of current gain (h_{21}) and Mason's unilateral gain (U) respectively. Both f_t and f_{max} were shown to be a function of gate and drain biases. For the Ti/Au ohmic HFET's, the best f_t was 46.9 GHz at $V_g = -3.2$ V and $V_{ds} = 9$ V for a 150-µm periphery device. The highest measured f_{max} was 103 GHz at $V_g = -4.6$ V and $V_{ds} = 16$ V for a 75-µm device (Figure 4) [1]. Both these devices had a gate length of 0.12 µm. Ti ohmic HFET's with a slightly longer gate (0.15 µm) demonstrated an f_t of 35.2 GHz.

Recent experiments have significantly improved the contact resistance. Using Ti/Al/Ti/Au sintered at 800°C for greater than 60 seconds, contact resistance of .60 Ω-mm have been achieved. Although devices will be fabricated using this method of forming ohmic contacts, they are not expected to achieve significantly better high frequency response, as explained below.

4. Discussions

Although the Ti/Au ohmic HFET's suffered from higher contact resistances, their RF performance actually compared favorably with that of the Ti ohmic devices. One reason was the shorter gate lengths achieved on the Ti/Au devices. Another reason was the decrease in magnitude of the drain-source impedance (Z_{ds}) as frequency increased, apparent in both the Ti/Au and Ti ohmic devices. The high contact resistance of these devices was actually shunted out by a parallel capacitive component as frequency increased, and this lowered the overall drain-source impedance significantly [1]. In this case although the Ti/Au HFET's had a higher drain-source impedance at DC than the Ti devices (~200 Ω as opposed to 100 Ω), Z_{ds} for both devices decreased to ~25 Ω at 26.5 GHz. This magnitude reduction of the drain-source impedance, together with the shorter gate lengths, made possible the superior RF performance of the Ti/Au ohmic HFET's.

5. Conclusions and Predicted Performance

MODFET's fabricated from AlGaN/GaN/SiC are expected to yield well over 10 W/mm at 10 GHz, based on the high breakdown electric field in the GaN (~4 MV/cm) and the high thermal conductivity of the SiC (~5 W/cm-°C). Based on our frequency response of short-gate MODFET's, the average electron transit velocity reaches at least 1.25 x 10^7 cm/s, showing excellent prospects for microwave, and even millimeter wave, frequency response. These power devices will operate at high voltage, high impedance, and even high temperature - 300°C. Thus they will become the microwave power amplifiers of choice for the rising wireless communication market of the future.

Acknowledgments

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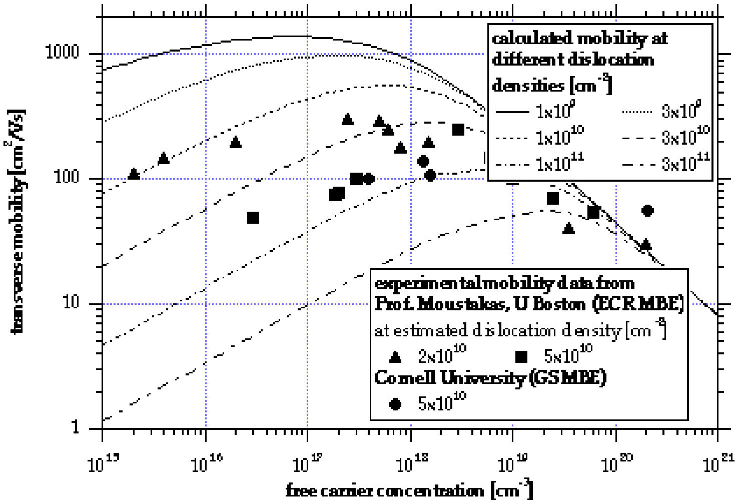

Figure 1. Transverse mobility as a function of carrier concentration and dislocation density

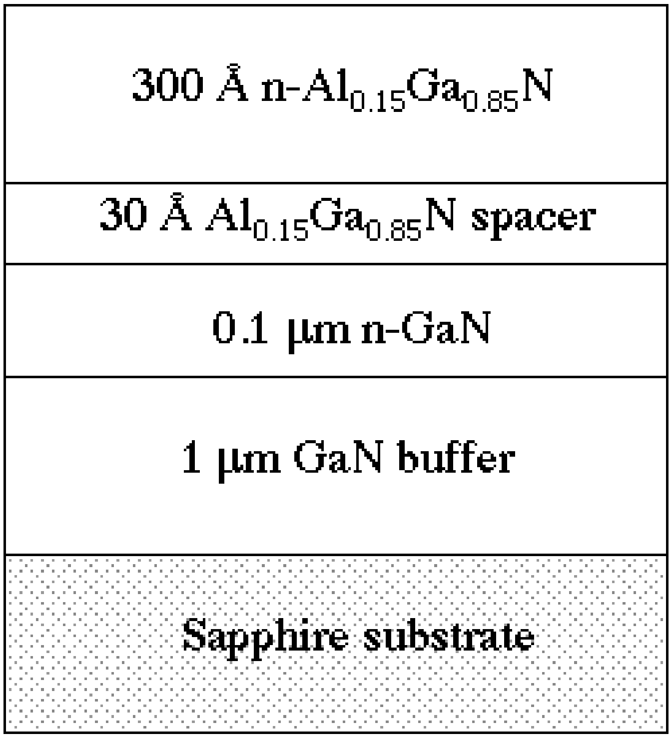

Figure 2. Layer structure of HFET wafer

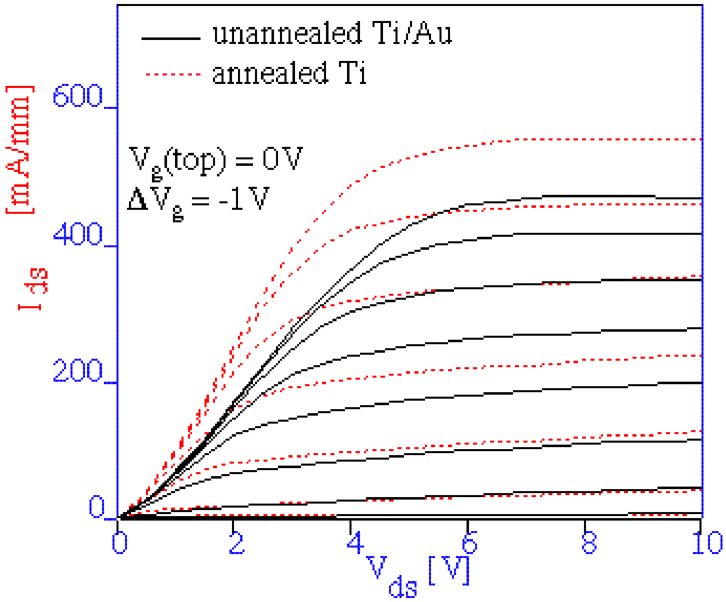

Figure 3. DC I-V characteristics of measured HFET’s

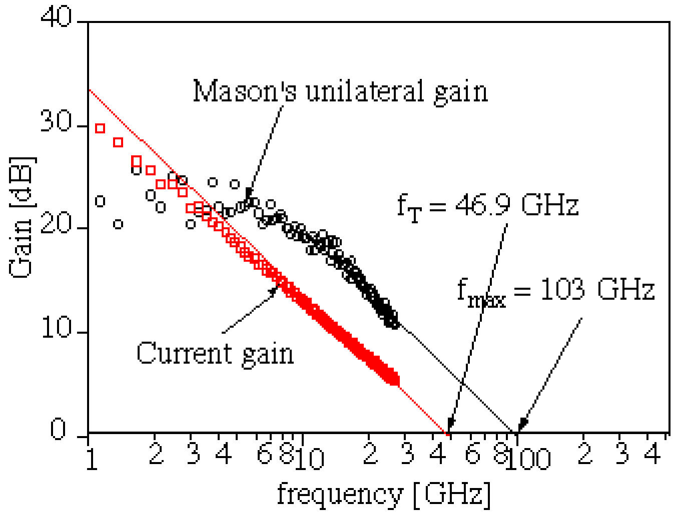

Figure 4. RF performance of Ti/Au ohmic HFET's

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