Backside Etching of GaAs Devices

Jeffrey A. Mittereder
Naval Research Laboratory, Washington, D.C.

The following is a technique for analyzing the area underneath a GaAs integrated circuit or discrete device which may aid in failure analysis. This procedure has been used in the past by the microelectronics community, and it is reviewed here for GaAs monolithic microwave integrated circuits (MMICs) and discrete devices. Because it is a destructive method, we use it in our lab after all other testing is completed. The substrate thickness of the GaAs is ~4 mils (25 μm).

1. First of all, the top side of the field effect transistor (FET) based MMIC is photographed to identify the failure sites, optically or with an SEM, as shown in Figure 1.

2. Next, if the device is die attached by eutectic solder, the circuit is removed from the package by delicately using tweezers while slightly heating the package. Sometimes we have a processing lab do this for us. This procedure is tough for discrete devices due to their small size. We have not attempted this on epoxied devices, although heating may be applicable.

3. The circuit is placed face down on an SEM sample holder, and then cold mounted in epoxy as shown in Figure 2 (a) and (b). The double-sided carbon tape keeps the metallization pattern intact, and also decreases specimen charging while imaging with an SEM.

4. When the cold mount is dry, the Au-Sn back side metal (which is usually silver colored) is sanded off; sanding is stopped when the substrate is reached (usually dark colored). 400 grit sandpaper works fine.

5. The GaAs substrate is then etched using 4 parts hydrogen peroxide, 1 part ammonium hydroxide. The etching progress is checked every 5-10 minutes under an optical microscope. It is stopped when the metallization pattern is revealed and/or the substrate is removed in the area of interest - Figure 3.

The top of Figure 3 shows the gate line shorted to the source, a feature which was underneath the air-bridge. The bottom of Figure 3 shows the source shorted to the drain. This view was not visible from the top of the failed circuit - Figure 1. The backside etching technique can most likely be used for silicon devices as well as with a change in the substrate etch (step 5). ■

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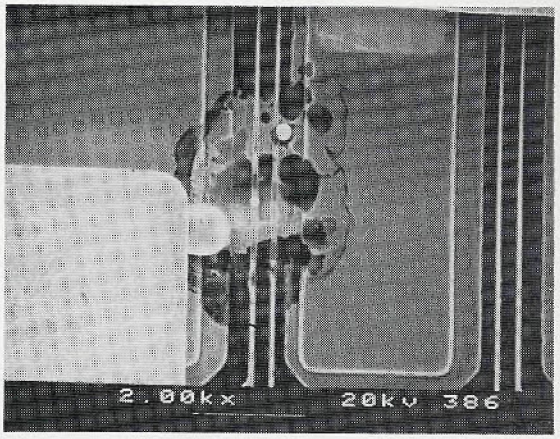
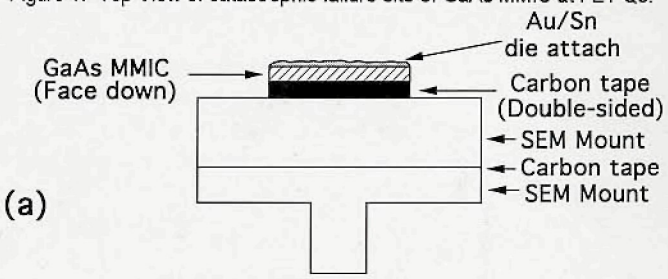


Figure 1: Top View of catastrophic failure site of GaAs MMIC at FET Q3.



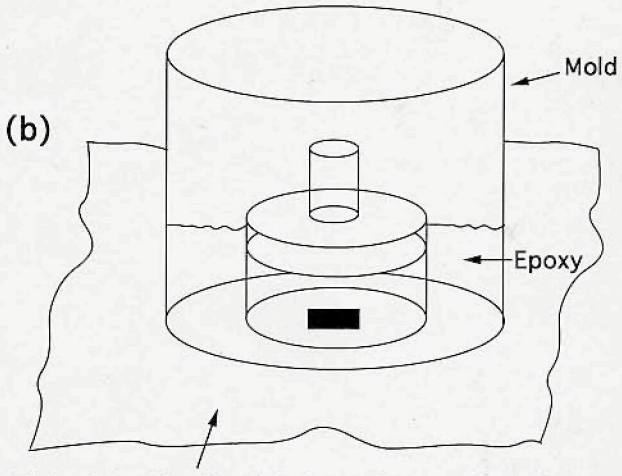


Figure 2: Mounting of GaAs MMIC.

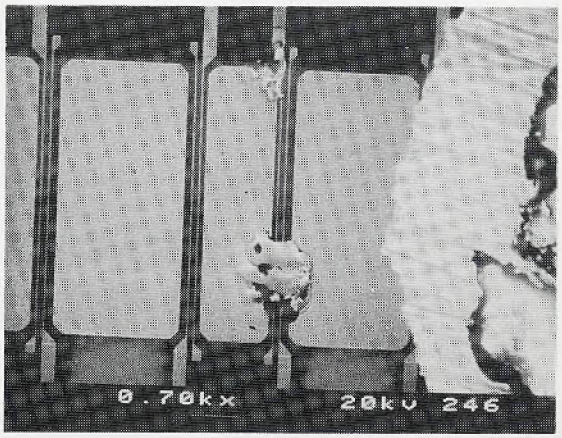


Figure 3: Backside view of failure site from Figure 1. This view reveals features not noticeable in the top view

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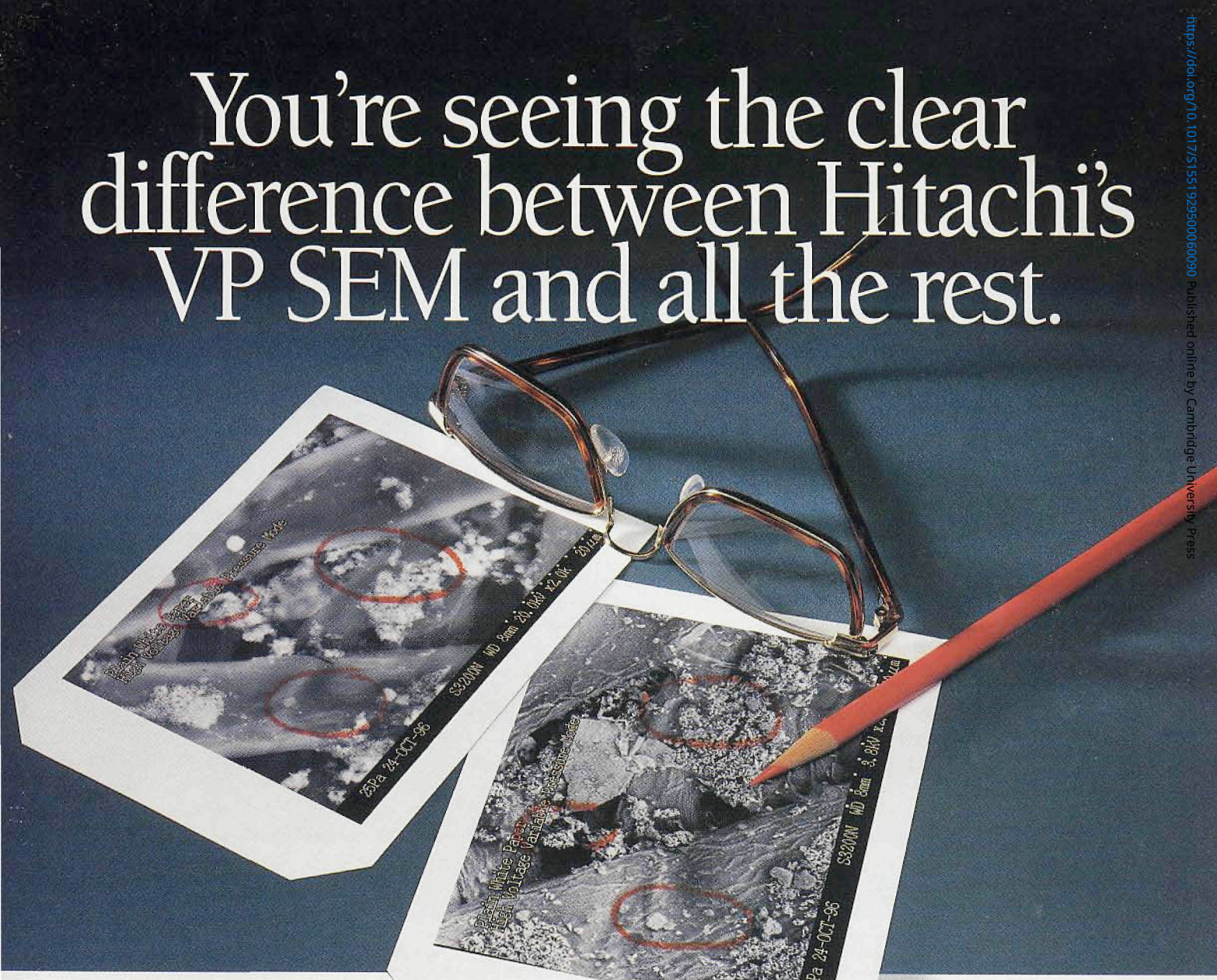

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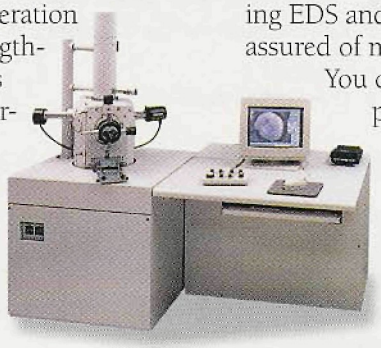

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