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120 GHz microstrip power amplifier MMICs in a commercial GaAs process

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Abstract

Single-ended and balanced 90–120 GHz microstrip power amplifier MMICs have been designed for cost-sensitive 5G and 6G backhaul in a commercial 6-inch, 0.1-μm GaAs process. At 108 GHz, measured output power is 20.4 and 22.5 dBm, respectively. At 120 GHz, measured output is 12.6 and 17.4 dBm, respectively. This is the highest reported for GaAs, among the highest reported to date for microstrip MMIC amplifiers at these frequencies and competitive with more expensive InP and GaN processes. Measurement is compared with simulation.

Introduction

Spectrum for high-capacity mobile backhaul applications from 92 to 114.25 GHz (commonly referred to as W-band) has been released to facilitate multi-gigabit wireless backhaul capacities for 5G and 6G [1–4]. As in the existing allocations at lower frequencies, cost and performance remain critical for the new allocation prompting the need for advanced power amplifier (PA) technology in a cost sensitive process [5, 6].

Promising results at 110 GHz, and beyond, have been obtained using coplanar waveguide design in InP, GaAs, and GaN [7–14]. This technology is attractive due to the simplified fabrication process. However, for a given semiconductor technology, microstrip typically provides greater power [13, 14].

In this paper, we present design and measurements of a pair of 90–120 GHz microstrip medium-power MMIC amplifiers, one single-ended and one balanced, fabricated using a 150-mm commercial GaAs pHEMT process. Our aim is to determine the high-frequency limits of microstrip GaAs PAs.

The paper is organized as follows: Section "Process and Amplifier Design" describes the GaAs process, and discusses transistor modeling, amplifier simulation, and design. Measurement methodology and results are presented in "Measured Results" section. These results are discussed and compared with other results in the literature in next section before some concluding remarks are made in following section.

An earlier version of this paper was presented at the 2022 European Microwave Integrated Circuit Conference, Milan, and was published in its Proceedings [15].

Process and amplifier design

Process

The process used for this work is the latest generation 0.1 μm GaAs pHEMT platform from WIN Semiconductors, PP10-20. This production technology on 150-mm wafers is optimized to support power and low noise applications through D-band and is qualified for 4 V operation. The PP10-20 transistor uses an electron beam defined 0.1 μm T-shaped gate, has typical f_t and f_{max} of 160 and 240 GHz, respectively, and 8 dB gain at 100 GHz for a 2 × 25 μm microstrip device. The process uses a 50 μm final substrate thickness, 565 pF/mm^2 capacitors, two front side interconnected metals and offers optional DC/RF isolated through-substrate via holes for low-inductance RF transitions.

Transistor modeling

Designing at a significant fraction of f_t requires care in the transistor device model. At these high frequencies, coupling becomes significant. The approach adopted here enables (i) non-standard, non-Process Design Kit device geometries to be used and (ii) the circuit electromagnetic (EM) simulation to consider the device metallization and surrounding matching circuitry as one.

The single-finger modeling approach is used to address this issue [16]. It allows the transistor's metal structure to be treated as part of the overall metallization, while the transistor's active semiconductor region is modeled separately.

To extract the intrinsic semiconductor region, simple 2×25 µm test transistors were measured up to 50 GHz. Our MQFET model [17] is fitted to the measured, extracted IV, and 50 GHz S-parameters over bias. Extracted correctly [18], the resulting model, when used with the single-finger approach, extrapolates to different device sizes and to the high frequencies used here. The model was checked for proper scaling with respect to transistor width and number of gate fingers with fresh S-parameter data measured to 110 GHz.

Amplifier simulation

The amplifier was designed in small sections using standard microstrip elements then gradually incorporated into a full two-and-a-half-dimension EM simulation of the circuit. Figure 1 illustrates the full EM of the circuit and a close-up of a pair of output transistors modeled using the internal (gap) differential source-gate and drain-gate port technique [16].

Microstrip PA design at these frequencies is challenging as the 50-µm substrate thickness becomes a significant fraction of a wavelength at the harmonics generated by the transistor's non-linear response. At 115 GHz, the substrate thickness is around 7% of the dielectric wavelength. At the third harmonic, it approaches a quarter wavelength and excitation of the dielectric transverse magnetic (TM) mode near 380 GHz [19]. In this work, only three harmonics were used in the circuit analysis instead of five as commonly used at lower frequencies.

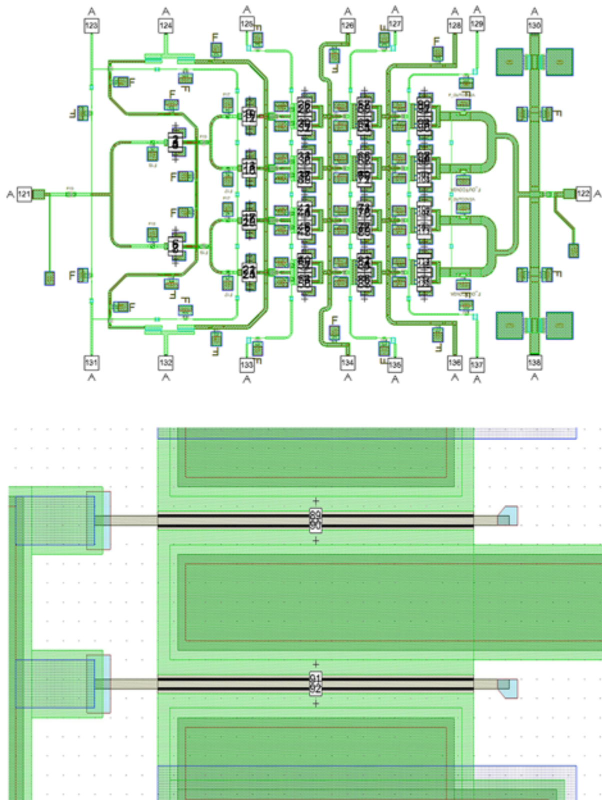

Figure 1. Upper: Core of the single-ended amplifier in Cadence Axiem EM software. The FET model is attached to the metallization using internal (gap) ports. Lower: Zoom in on part of the upper right FET in the output stage showing the internal (gap) differential source-gate and drain-gate ports.

Amplifier design

Two 90–120 GHz amplifiers have been designed. The core design is a five-stage single-ended amplifier with gate and drain biases for stages 1A and 1B connected to common gate and drain external pads, creating for the user a four-stage amplifier – see Fig. 2. The transistor peripheries are as follows, with the larger FET models extrapolated from the base device:

Stage 1A: two 2×25 µm FETs = 100 µm,
Stage 1B: four 2×25 µm FETs = 200 µm,
Stage 2: four 4×20 µm FETs = 320 µm,
Stage 3: four 4×30 µm FETs = 480 µm, and
Stage 4: four 4×40 µm FETs = 640 µm.

The nominal bias of 250 mA/mm is obtained from a 4 V drain supply with a gate bias of −0.3 V. A conservative approach was initially taken as this was the first use of a new transistor model and the first design in a new semiconductor process.

Virtual, internal open circuits are realized in stages 1B, 2, 3, and 4 with open circuit bias lines, terminated with resonated short-circuits at center-band, supplying dc. Large de-Q'ed capacitors are incorporated into the bias supply lines that dampen low frequency gain. Matching circuits use cap-on-via to improve performance and transistor layouts with the maximum number of backvias were chosen to reduce source inductance.

An E-band PA in the same core process, with similar, small, device widths, maximum backvias, and the same dc power density of 1 W/mm was estimated to have 137°C gate temperature averaged to spot diameter of 8 µm with a backplate of 85°C [20]. This amplifier is expected to heat similarly.

Amplifier stability was confirmed using Rollett's k-factor [21] and Ohtomo's loop analysis [22]. Attention was paid to the shared bias of stage 1 and odd-mode operation for stages 2–4.

The single-ended MMIC1 layout is symmetric to facilitate construction of the second, balanced design, MMIC2, to increase the output power (Fig. 3). The Lange couplers were carefully constructed to maintain performance on the 50-µm substrate while adhering to the design rules.

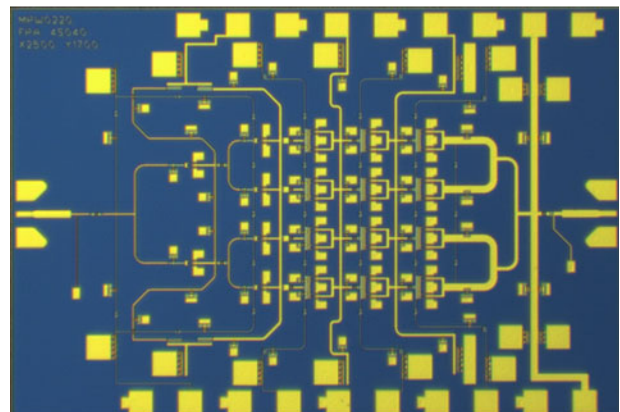

Figure 2. Single-ended amplifier, MMIC1. The area is $2.5 \times 1.7 = 4.25$ mm^2.

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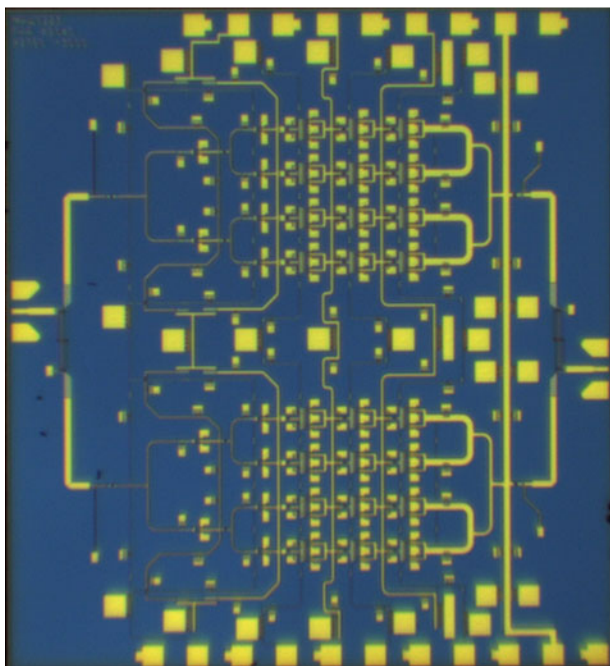

Figure 3. Balanced amplifier, MMIC2. The area is 2.75 × 3.0 = 8.25 mm^2.

Measured results

Vector measurements

The S-parameters were measured with an Anritsu VectorStar, using on-wafer structures for calibration. The measured gain and return losses are plotted in Fig. 4 for both the single-ended and balanced PAs. The simulated gain is also shown for the single-ended case.

The gain of the single-ended and balanced amplifiers is very similar and exceeds 15 dB from about 82 to 118 GHz. The input return loss is significantly improved by the input Lange coupler as expected; however, the output return loss is only improved for some frequencies and at others it is worse, perhaps due to coupling from adjacent drain lines.

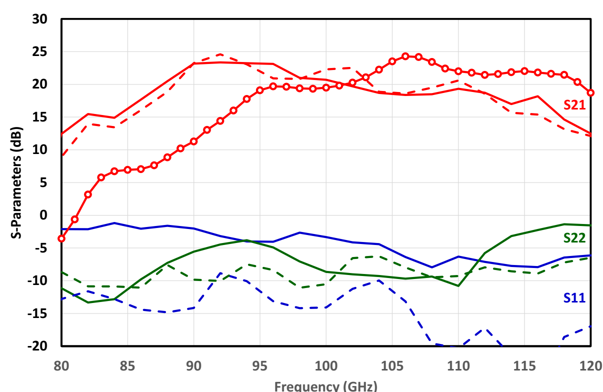

Figure 4. Measured S-parameters for the single-ended (solid lines) and balanced (dashed) PA: S11 (blue), S21 (red), and S22 (green). Vd = 4 V and Vg = −0.3 V. Simulated S21 for the single-ended PA also shown (red, solid line with circles).

Scalar measurement methodology – WR6.5 and WR10

The scalar measurements used two different set-ups, W-band, below 110 GHz, using WR10 waveguide, and D-band, above 110 GHz, using WR6.5 waveguide. Both used Virginia Diodes Inc. (VDI) SGX series multipliers: times six for 75–110 GHz and times twelve for 110–130 GHz measurements. The former is specified as having 10 dBm minimum, 14 dBm typical output power, while the latter is specified as having 3 dBm minimum, 8 dBm typical, output power.

As more power was available at W-band, the W-band measurement input side waveguide assembly included an isolator, manual level setting attenuator and a directional coupler (with a Keysight W8486A waveguide power sensor at the couple port) between the source and the input side waveguide probe. At D-band, because the available input power was much lower and waveguide losses higher, two sets of power measurements were made: (i) over a lower input power range with a manual attenuator and directional coupler so the input power could be varied and monitored, and (ii) at a fixed, maximum possible input power.

At W-band, the output power was measured using a second Keysight waveguide power sensor. At D-band, a VDI Erikson PM5 power meter and sensor was used. This power meter is specified for operation from 75 to greater than 3 THz. The sensor uses WR-10 waveguide and tapers are available for waveguide bands above this. The total waveguide loss of the waveguide ahead of the power sensor taper must be accounted for in the measurement results. When using the W-band to D-band taper, this loss is 0.31 dB.

The measurement calibration was made in three steps. First step was to measure the power at the end of input side waveguide. At W-band, both the power at the input to the input probe and at the power at the directional coupler coupled port, were measured; at D-band, only the power at the input to the input probe was measured. The output side waveguide assembly was then added to the input side waveguide, and the power at each frequency again recorded. From this, the loss of the output side wave assembly was derived. Then, the waveguide assemblies were connected to their input and output probes, probed down on a wafer through, and the frequency steps repeated. The input probe plus through plus output probe loss was then calculated using the previous measurements. Half this loss value was then assigned to the input side, and half to the output. From these measurement steps, the power at the circuit's input and output can be derived during the measurement. Doing the calibrations in this order meant that the waveguide connections are were not disturbed between calibration and measurement, improving the measurement integrity.

For the lower input power measurements, D-band isolators were included between the directional coupler through port and the input probe, and between the coupled port and a Keysight W8486A W-band power sensor used for input power monitoring. This ensured that the directional coupler ports saw constant D-band impedances during both calibration and measurement, despite there being a W-band-D-band mismatch at the power sensor connection. The Keysight power sensor calibration value for 110 GHz was used for all measurements, with the calibration difference between the Keysight power reading and the Erikson power meter then used to determine the input power to the circuit during measurement. For the higher input power measurements, the manual attenuator and directional coupler were removed, and the full, available input used throughout.

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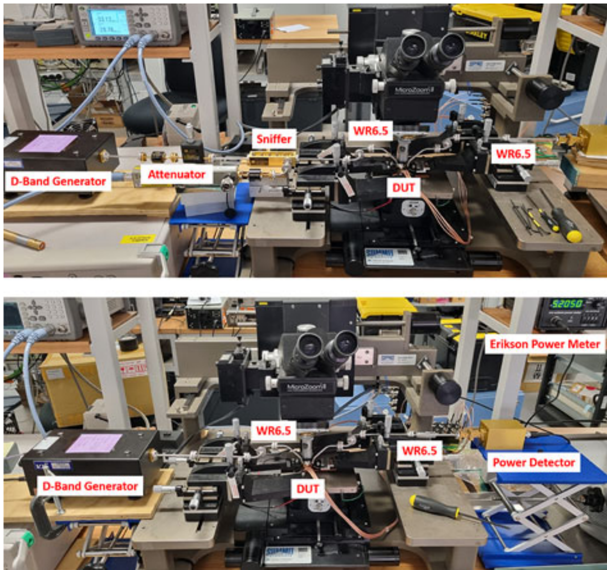

Figure 5. Upper: Full WR6.5 measurement set-up with variable attenuators and sniffer. Lower: Striped down set-up without these for maximum input power.

The D-band (WR6.5) measurement set-up is illustrated in Fig. 5. The W-band (WR10) set-up is similar. The RF probes are 100 μm waveguide Picoprobes from GGB.

Measured results – W-band (WR10)

The measured W-band output power is shown in Fig. 6 as a function of frequency at three gate biases, −0.5, −0.4, and −0.3 V, at the input level shown in the inset. Simulated value is also shown.

As with the S-parameter simulation, the transistor model has not been refitted to FET data from the amplifier's wafer nor has any other parameter been adjusted such as MIM capacitance value (i.e. SiNx thickness). The simulation is the original design prediction based on measured 50 GHz 2 × 25 μm S-parameter data. Based on Figs. 4 and 6, the discrepancy between measurement and simulation is a shift of about 5 GHz. The gain and power levels are in good agreement.

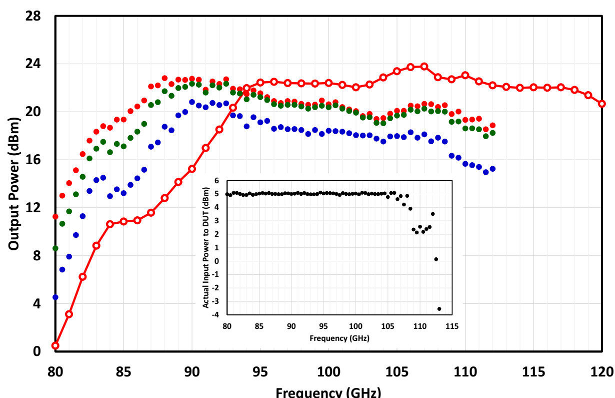

Figure 6. Output power for the single-ended PA, MMIC1, at 5 dBm wanted input power. Vd = 4 V; Vg = − 0.5 V (blue), −0.4 V (green), and −0.3 V (red). Red, solid line with circles is simulation for − 0.3 V. Actual power at the DUT when 5 dBm is the wanted input power is shown in the inset—it falls rapidly above 108 GHz with the W-band (WR10) experimental set-up.

Measured scalar gain, output power, and power-added efficiency (PAE) for the single-ended amplifier at 108 GHz are shown in Fig. 7 for gate biases −0.5, −0.4, and −0.3 V. The P1dBs are, respectively, 12.9, 16.5, and 17.4 dBm. The P3dB point was not reached for the −0.5 V gate bias but is 18.7 dBm for both higher biases and the maximum output power is 20.4 dBm. The maximum PAE is not reached. The value measured here varies between 4.4% and 5.3%.

Figure 8 shows the measured power and PAE of the balanced amplifier. The output power reaches 22.5 dBm at 108 GHz and exceeds 20 dBm from 86 to 112 GHz. Figure 9 shows the data vs input power. The P1dB for the −0.3 V bias is 21.0 dBm and the P3dB is 22.3 dBm; both 3.6 dB higher than single-ended case. Again, the maximum PAE is not reached but exceeds 4.1%.

The Lange couplers used in the balanced amplifier have performed well despite the high frequency and thin substrate. There is little loss to the measured gain and the balanced P1dB and P3dB are a little more than 3 dB higher than in the single-ended case. We suggest that the load-presented to core amplifiers by the Lange coupler in the balanced case provides a better power match than provided by the measurement probe and instrumentation in the single-ended case.

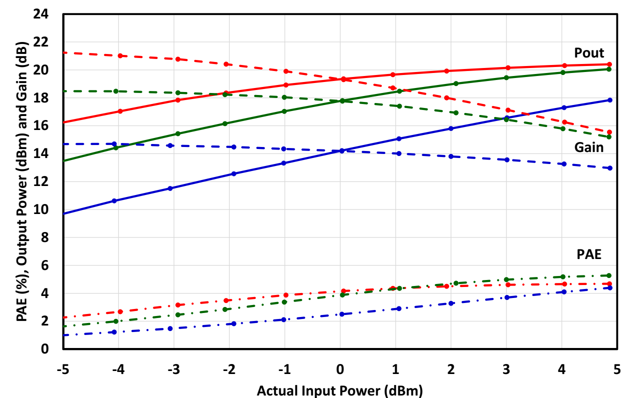

Figure 7. 108 GHz single-ended, MMIC1, measured output power (solid), gain (dashed), and PAE (dot-dash) vs input power. Bias: Vd = 4 V; Vg = − 0.5 (blue), −0.4 (green), and −0.3 V (red). Dots mark exact measurement points.

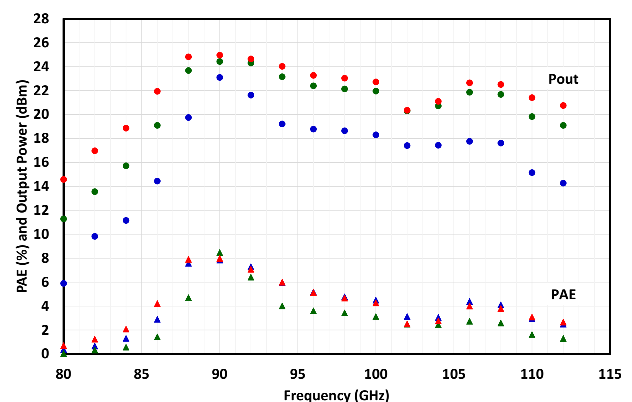

Figure 8. Output power (circles) and PAE (triangles) for the balanced PA, MMIC2, at 5 dBm wanted input power (see Fig. 2). Vd = 4 V and Vg = − 0.5 V (blue), −0.4 V (green), and − 0.3 V (red).

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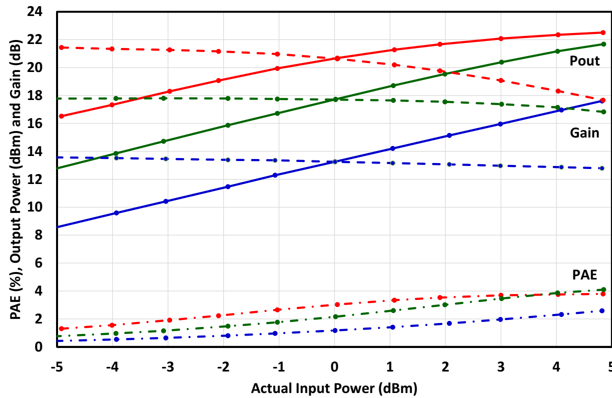

Figure 9. 108 GHz balanced, MMIC2, measured output power (solid), gain (dashed), and PAE (dot-dash) vs input power. Bias: Vd = 4 V; Vg = −0.5 (blue), − 0.4 (green), and −0.3 V (red). Dots mark exact measurement points.

Measured results – D-band (WR6.5)

Only a modest range of input powers were achievable under attention control with the WR6.5 (D-band) system, so an additional maximum input power point is added by removing the input power coupler and sniffer. This extends the available input power from approximately −8 dBm at the DUT to 0–4 dBm. Figure 10 shows the measured 110–120 GHz gain and output power as the input power is controlled plus at an additional maximum input power point. Clearly, MMIC1 begins to compress before this final input power level is reached.

The optimal bias is explored in Figs. 11 and 12, where it is determined that a lower drain bias, such as Vd = 2.5 V, and higher gate bias, such as Vg = −0.1 V, maximizes output power at these higher frequencies. This improved 120 GHz performance at the lower drain potential/higher current biases may be due to the higher gain in intermediate stages at the lower drain/higher current bias.

Figure 13 plots the output power of MMIC1 and MMIC2 at this optimal bias of Vd = 2.5 V and Vg = −0.1 V as a function of frequency for the maximum achievable input power. At 120 GHz, the output power is 12.6 dBm with a PAE of 1.2% for MMIC1 and 17.4 dBm with a PAE of 1.8% for MMIC2. The modest saturation exhibited in Fig. 10 suggests that higher powers are achievable for both MMICs, and similarly the maximum PAE value may be achieved at a different input power level than the maximum experimental input power achieved here. The 5.8 dB difference between the output powers of MMIC1 and MMIC2 at 120 GHz is presently unexplained.

The 120 GHz output power levels are less than expected from the initial single-ended simulation in Fig. 6 despite the input difference, i.e. 20.7 dBm simulated with 5 dBm input power compared with 12.6 dBm measured with 1.85 dBm input power. This may be due to inaccuracies with the scalable model. It may also be a result of only simulating to the third harmonic or the influence of the dielectric TM mode on higher harmonics.

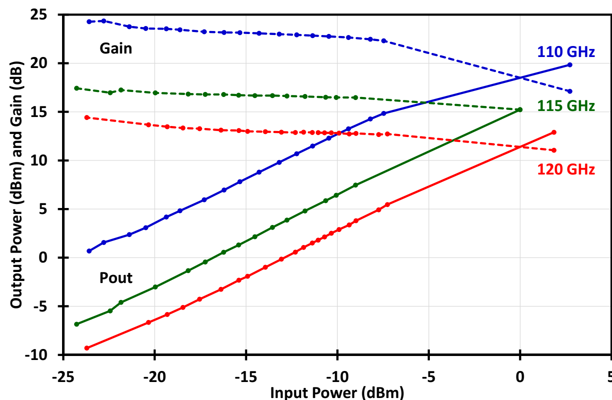

Figure 10. MMIC1 output power and gain vs input power at 110 (blue), 115 (green), and 120 GHz (red). Bias: Vd = 4 V; Vg = − 0.2 V.

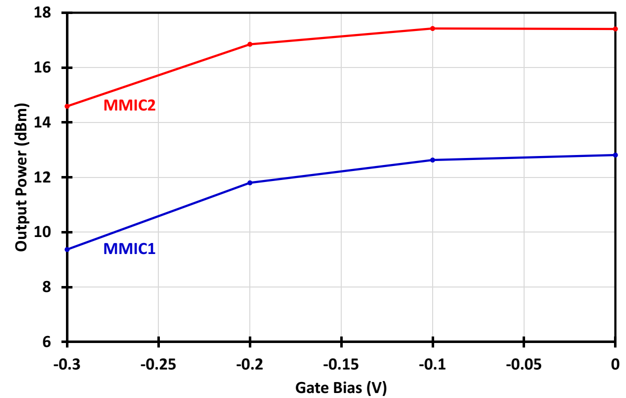

Figure 11. 120 GHz MMIC1 and MMIC2 output power vs gate bias. Vd = 2.5 V.

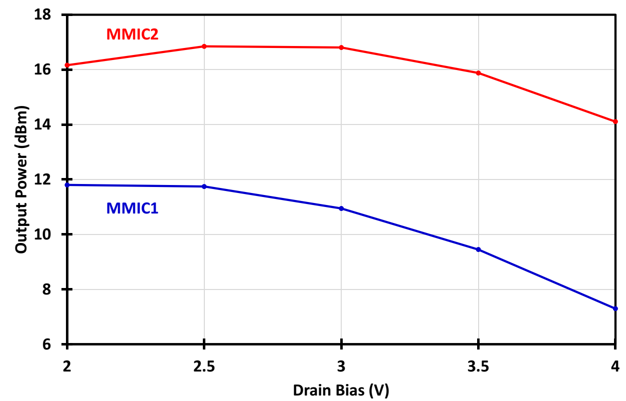

Figure 12. 120 GHz MMIC1 and MMIC2 power vs drain bias. Vg = − 0.2 V.

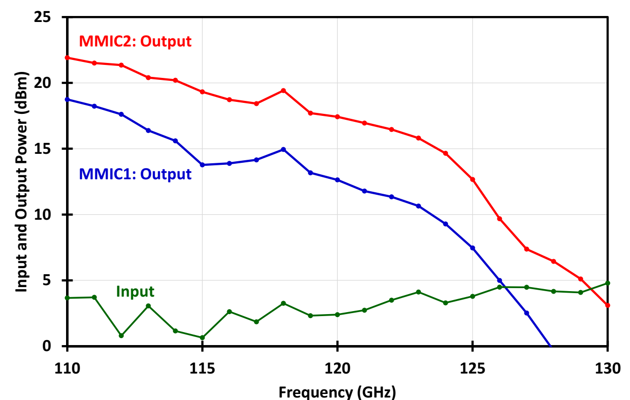

Figure 13. MMIC1 (blue) and MMIC2 (red) output power vs frequency at maximum achievable input power (green) in our laboratory with this D-band (WR6.5) experimental set-up. Bias: Vd = 2. 5 V and. Vg = − 0.1 V.

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Comparison and discussion

The work presented here is compared with selected state-of-the-art microstrip and coplanar GaAs, InP and GaN FET amplifiers at 120 GHz in Table 1.

The cascode coplanar designs in [7] were fabricated on an earlier generation of the WIN PP10 process used here. The reference does not report the power at 120 GHz; however, the 7–8 dBm reported at 138 GHz is likely to be similar at 120 GHz given the flatness of the gain.

In [8], the coplanar design fabricated at HRL obtains more than 9 dB of gain and 14–16 dBm of output power over 70–140 GHz from a 100-nm InP process. The authors report a left shift between simulated and measured gain of about 10 GHz.

The higher breakdown and, hence, drain bias of GaN PAs is associated with enhanced PAE, although this may be reduced in practice by higher knee voltage and knee walkout.

The F-band, 5-stage cascode CPW design from Raytheon in [9] achieves an output power of 17.4 dBm and PAE of 4.3% at 120 GHz but these metrics are not reported for other frequencies. The measured gain roll-off either side of 120 GHz suggest that both the output power and PAE may be reduced.

The gain of the four-stage, 100-nm GaN cascode CPW design in [10] peaks strongly at 110 GHz; however, the reported saturated output power is relatively flat, varying from 18.2 dBm at 105 and 18.5 dBm at 120 GHz to 20.3 dBm at 115 GHz. The PAE varies from 1.4% at 105 GHz to 1.7% at 120 GHz, peaking at 2.6% at 115 GHz.

The cascode CPW design in [11] is fabricated on a shorter 70 nm gate length GaN process. It achieves output power above 22 dBm and PAE of 10%, or better, from 89 to 123 GHz. The measured S-parameters and power are in good agreement with simulation.

The D-band 100-nm GaN cascode CPW design reported in [13] has more than 25 dB of gain from 107 to 148 GHz. Excellent output power, 26.5 dBm at 15 V and 25.0 dBm at 10 V, and PAE, 11.5% and 16.5% respectively, are reported at 120 GHz. However, the output power and PAE match fall away sharply at other frequencies with the PAE dropping to near 1%.

The common source, microstrip GaN designs reported by Quinstar, and fabricated by HRL, in [14] exhibit excellent output power and leading PAE over a broadband of 102–118 GHz for their D1 design and 98–122 GHz for D2. The authors compare the measured and simulated S-parameters with the simulations in reasonable agreement although some frequency left shift, lower gain, and unsimulated gain notches are observed.

The PAs presented here, fabricated on a commercial 6-inch process, produce the highest power yet reported by GaAs MMICs at 120 GHz. Furthermore, they produce comparable gain, power, and PAE to designs in more expensive processes, such as InP and GaN across the 90–120 GHz range.

Table 1. Selected microstrip and coplanar 120 GHz FET amplifiers

Frequency (GHz)	Gain (dB) at 120 GHz	Psat (dBm) at 120 GHz	PAE (%) at 120 GHz	Area (mm^2)	Architecture	Technology	f_t/f_{max} (GHz)	Foundry	Ref.
100–150	12 (11)	7[a] (8[a])		0.72 (2.1)	Un(balanced) 4-stage cascode coplanar	100-nm pHEMT on 50 μm GaAs	130/180	WIN	[7]
65–140	9	15		1.68	3-stage grounded coplanar	100 nm InP HEMT		HRL	[8]
115–125	18.9	16.8	4.3		5-stage microstrip	150 nm GaN HEMT on 50 μm SiC		Raytheon	[9]
105–120	27	18.5	1.7[b]	3	4-stage cascode coplanar	100-nm GaN on 75 μm SiC	110/280	Fraunhofer	[10]
80–122	25	22.5	10	3.5	5-stage coplanar	70-nm GaN on 75 μm SiC	145/296	Fraunhofer	[11]
110–145	29	26.5 (15 V) 25.0 (10 V)	11.5 (15 V)[c] 16.5 (10 V)[c]	7.5	4-stage cascode coplanar	100-nm GaN on 75 μm SiC	100/300	Fraunhofer	[13]
98–122 (D2)	21.2 (D1) 17.5 (D2)	24.7 (D1) 25.3 (D2)	6.0 (D1) 4.3 (D2)	7.0 (D1) 6.4 (D2)	4-stage microstrip	140-nm GaN on 50-um SiC	85/220	HRL	[14]
90–120	19.5	12.6	1.2[d]	4.25	5-stage microstrip	100-nm pHEMT on 50 μm GaAs	160/240	WIN	Here, MMIC1
90–120	20.5	17.4	1.8[e]	8.25	Balanced 5-stage microstrip	100-nm pHEMT on 50 μm GaAs	160/240	WIN	Here, MMIC2

[a]138 GHz (Pin = 0 dBm).
[b]PAE = 1.4–2.6% over 105–115 GHz.
[c]PAE = 1–5% elsewhere.
[d]5% at 108 GHz.
[e]3–8% for 90–112 GHz.

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Conclusion

A single-ended and a balanced 90–120 GHz microstrip PAs have been designed in a new, commercial 150-mm (6-inch), 0.1-μm GaAs process for cost-sensitive W- and D-band communications applications.

At 108 GHz, measured output power is 20.4 and 22.5 dBm, respectively. At 120 GHz, measured output power is 12.6 and 17.4 dBm, respectively. Good agreement with original simulation has been shown for the lower, W-band, range, but the agreement is poorer for D-band.

These output powers and PAEs are the highest reported for GaAs and among the highest reported to date for microstrip amplifiers at these frequencies. Fabricated in an inexpensive, commercial, 6-inch GaAs pure-play foundry, they are competitive with circuits fabricated in high-cost InP and GaN processes at non-commercial, restricted foundries.

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Author contributions. S.J.M. led the circuit design, data analysis, and paper writing. M.G.M. designed and implemented the circuit measurement. J.M. and M.C.G. made significant contributions to the circuit design. A.E.P. developed the transistor model and M.C.H. provided project guidance and funding.

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Competing interests. The authors report no conflict of interest.

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