

EFTEM Mapping of Copper - Porous SiLK Structures

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SiLK is a thermoset spin-on aromatic hydrocarbon polymer, manufactured by Dow Chemical, which is being investigated as a low dielectric constant material for 0.13 μ m semiconductor technology and beyond [1, 2, 3, 4]. IBM employed dense SiLK, with a dielectric constant k of 2.65, in their 0.13 μ m copper technologies in early 2000 [2]. Comprised of an isotropic closed-pore network, porous SiLK (p-SiLK) has a k -value less than 2.2 and an average pore size of about 20nm [3, 4].

In the current study, energy-filtered TEM was used to examine the effect of an oxidizing versus a reducing etch on patterned p-SiLK, as well as the conformity of Ti and Ta barrier metals in contact with the etched p-SiLK and infiltration of the barrier metals into the dielectric. The test structures were single-level Cu damascene trenches. All images were recorded with an FEI Tecnai F30-ST FETEM, operating at 300kV and equipped with a 2kx2k Gatan Imaging Filter. TEM specimens were prepared on an FEI Strata 235 Dualbeam [5].

Zero-loss filtering was used to enhance the contrast of the pores relative to the dielectric matrix, as well as to more easily distinguish the nitride stop layer and nitride capping layer from the oxide and the p-SiLK (Figs. 1a,b and 2a,b). In addition to 3-element RGB overlays of elemental EFTEM maps, single-color overlays of individual elemental maps with the zero-loss filtered image were also used to more clearly show the location of elements in the structure.

Figure 1 shows unfiltered and zero-loss filtered images and EFTEM maps of a structure that received the oxidizing p-SiLK etch, followed by Ti barrier deposition, Cu seed deposition, and Cu fill. The p-SiLK along the sidewalls of the trenches was damaged, and the Ti from the barrier penetrated into the surrounding p-SiLK. Figure 2 shows unfiltered and zero-loss filtered images and elemental maps of a structure that received the reducing etch, followed by Ta barrier deposition, Cu seed deposition, and Cu fill. In this case, the p-SiLK along the trench sidewalls was much less damaged, and the Ta barrier did not penetrate into the surrounding dielectric.

As demonstrated by the Ta map in Fig. 2f, EFTEM mapping is not ideally suited to high energy loss elements. The Ta M_5 EELS peak is at 1735eV. At such a high energy loss, the signal-to-noise ratio is very low, making Ta difficult to map. In the Ta EFTEM map, a Ta signal erroneously appears in the Cu fill; however, no Ta incorporation occurred during Cu deposition. Diffraction contrast in the Cu also contributed to the EELS signal in the Cu. EELS or EDX line profiles in STEM mode correctly illustrated the location of the Ta barrier.

References

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- [2] P. Singer, Semiconductor International (May 2000).
- [3] J. H. Golden, et al., Semiconductor International (May 2001).
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- [5] The authors would like to acknowledge Sheila Morgan for preparing the TEM specimens.

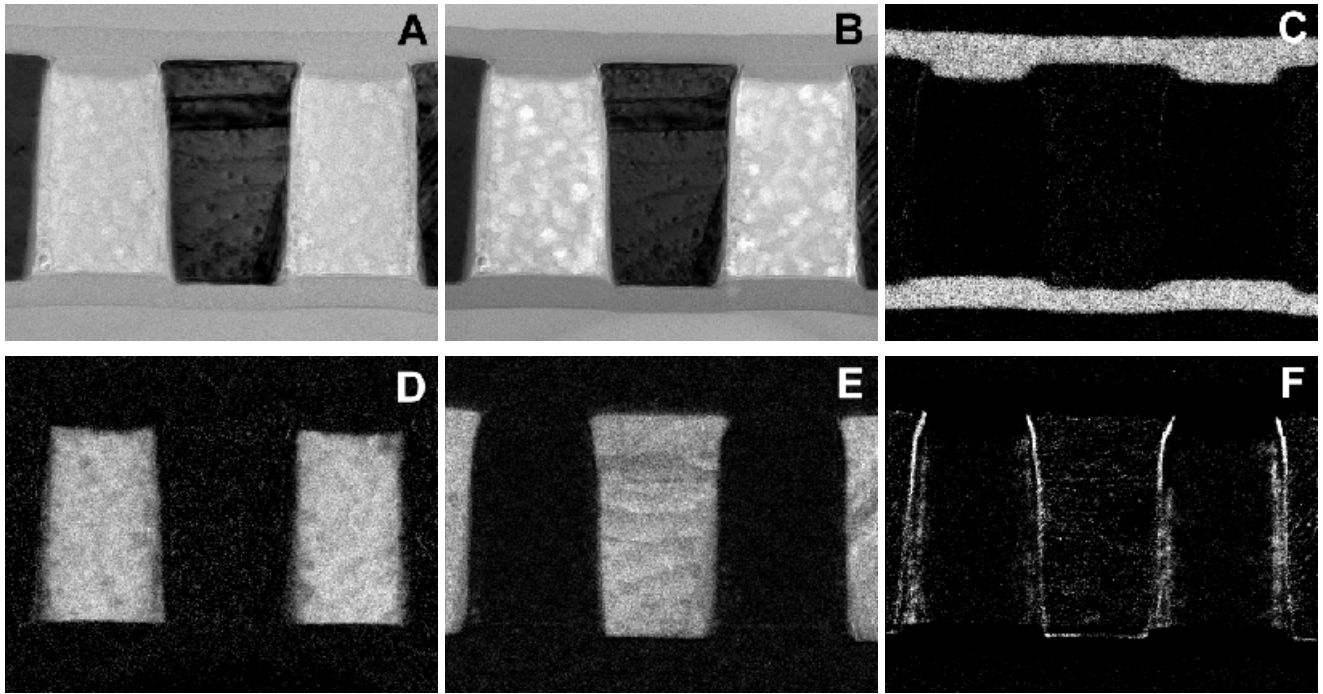


FIG 1. Oxidizing p-SiLK etch plus Ti barrier, Cu seed, and Cu fill: A) unfiltered brightfield, B) zero-loss filtered, C) nitrogen map, D) carbon map, E) copper map, and F) titanium map.

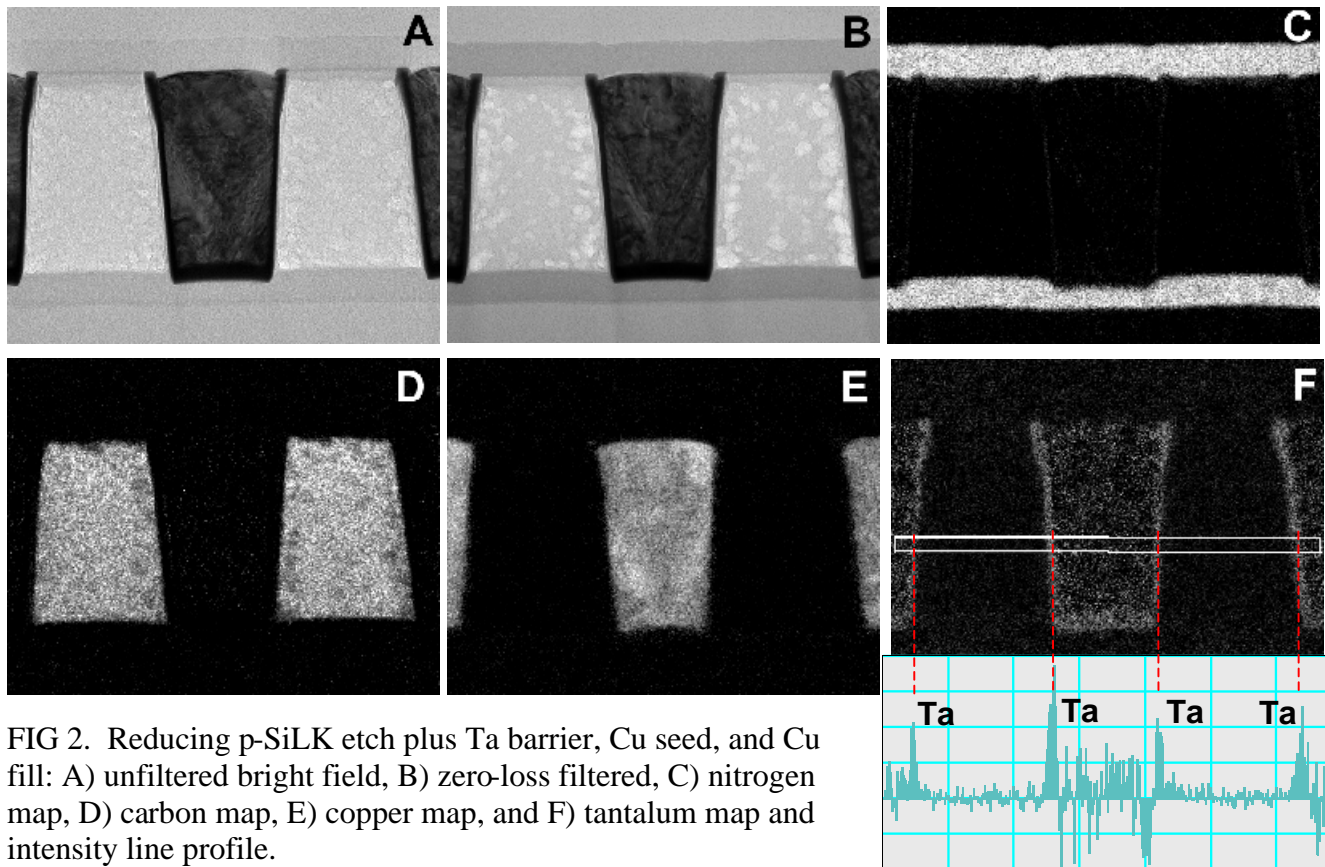


FIG 2. Reducing p-SiLK etch plus Ta barrier, Cu seed, and Cu fill: A) unfiltered bright field, B) zero-loss filtered, C) nitrogen map, D) carbon map, E) copper map, and F) tantalum map and intensity line profile.