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Issues Affecting Quantitative Evaluation of Dopant Profiles Using Electron Holography

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The semiconductor industry has a pressing need for information about dopant profiles. Reliable data is required for evaluation of process parameters and as input to simulations of dopant diffusion. Recent studies with electron holography have shown that 2-D dopant profiles can be successfully imaged with high-spatial resolution and sensitivity[1]. However, further research is needed to evaluate artifacts that prevent quantification on a routine basis.

Specimen preparation issues are perhaps the most troublesome. Special requirements for electron holography of semiconductor junctions include the presence of vacuum within a few hundred nanometers of the area of interest and a thickness profile that is predictable and independent of features of electrical interest such as gates and metallization layers. For bulk test samples, wedge polishing provides a good sample from which quantitative data can be extracted. For these samples, 100nm layers of protective materials such as TEOS or metal can be deposited on wafer prior to cross-sectioning and wedge-polishing. Wedge-polishing the sample at angles of 2° to 4° with progressively finer polishing papers produces a sample with uniform thickness profile as well as proximity to the vacuum edge of the sample. For example, see FIG. 1. These samples are generally cleaned using low-energy ion-milling to remove debris from the polishing and carbon coated to reduce charging. Quantitative evaluation of these samples has been successful in providing data on dopant diffusion and dopant activation in conjunction with simulations based on SIMS data[2].

Sample preparation using focused ion beam (FIB) with its highly controlled, site-specific capabilities would be preferable. However, disadvantages of this technique include uneven thickness or curtaining effects due to due to differential milling of metallization layers. This technique also produces samples with significant electrically “dead” surface layers that complicate quantitative evaluation[3]. Innovative approaches are currently being applied to overcome these drawbacks. In-situ lift-out, followed by FIB thinning from the Si-side of the device produces a sample without curtaining effects. The FIB is used to cut out a window through the top of the device to allow access by the vacuum reference wave for holography. The sample is further thinned from the backside to optimum thickness in a Ar ion mill to remove surface layers damaged by the FIB[4]. FIG. 2 shows such a TEM image and phase image.

Charging of samples during observation produces band-bending, junction biasing and fringing electric fields which may prevent quantitative evaluation. Grounding the sample to the grid, coating the sample with conductive coatings have been shown to minimize these effects, although careful quantitative analysis is needed to evaluate residual electrical disturbances [5].

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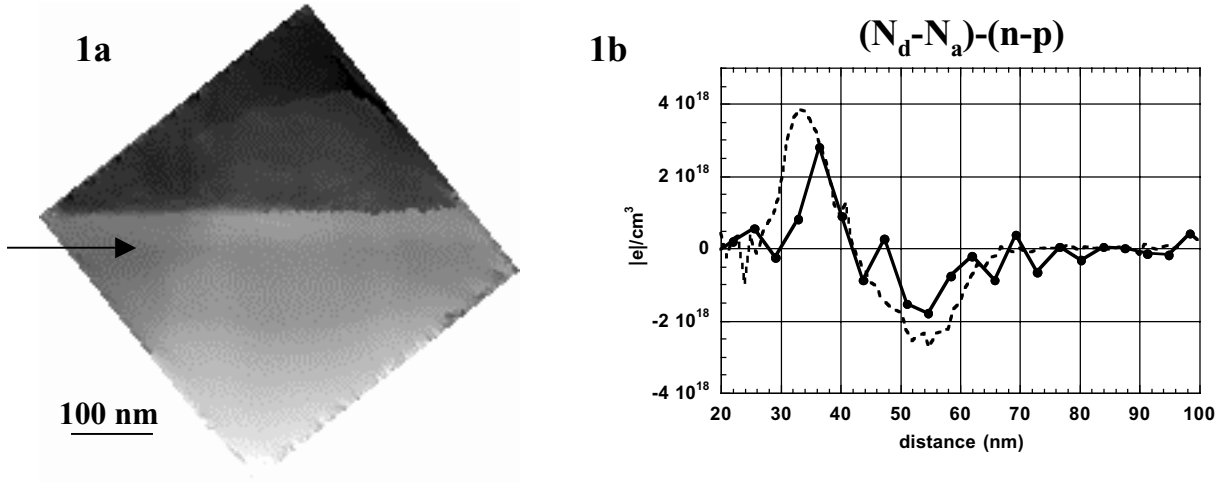

FIG. 1 a) Holographic phase image of ultrashallow junction (arrowed) produced by diffusion of P from spin-on glass. Sample prepared by wedge-polishing and Ar ion-milling. b) Comparison of electronic charge present in junction depletion region from holographic measurements (solid) and simulation (dotted) based on SIMS data indicates 70%-80% phosphorus activation.

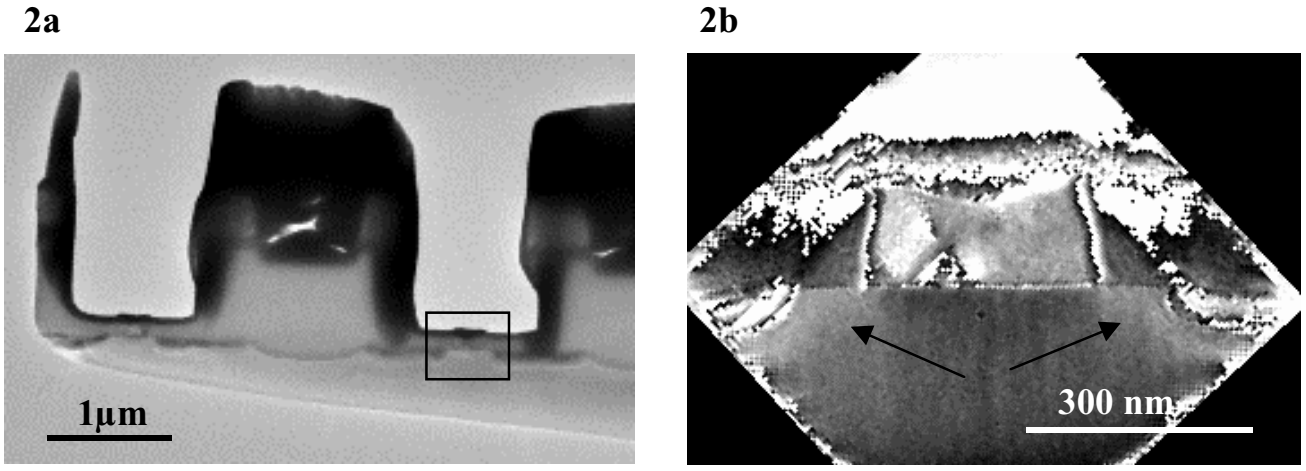

FIG. 2 a) TEM image of transistor devices prepared by INLO-FIB and backside thinning after further backside ion-milling. Area for hologram indicated. b) Reconstructed holographic phase image of transistor showing source/drain extension regions (arrowed) under sidewalls.

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