CNET Hosts First European Silicon on Insulator Workshop

The First European Workshop on Silicon on Insulators organized by the Société des Electriciens and Electroniciens de France and the Centre National d' Études des Télécommunications (CNET) de Grenoble was hosted at the CNET facilities from March 15 to 17, 1988.

Each day of the workshop centered around different subjects, one or two invited talks introducing each subject. The first day was devoted to zone melting recrystallization (ZMR) techniques (lamp, strip heaters, and laser) and porous silicon techniques. During the morning of the second day, all the materials aspects of the SIMOX technique were presented. After a tour of the CNET laboratories and pilot line, a poster session was held. This was a key moment of the meeting with excellent contributions that sparked stimulating and animated discussions. The third day was devoted to electrical measurements on devices fabricated using the different SOI techniques. The workshop closed with a roundtable and discussions between the panel and the audience.

The workshop was acceded a success by the 140 participants, who appreciated the high quality of the technical sessions and the organization. Participants from the European countries, the United States, Japan, and the USSR were still present even for the last paper. A friendly atmosphere contributed to many informal discussions and contacts. The next European workshop will be held in England.

Several conclusions can be drawn from this workshop:

1. There is no single SOI material to fulfill all the proposed applications.
2. The bulk silicon competitor in the submicron ULSI technology will be an SOI structure with a very thin active layer. SIMOX and porous silicon appear to be the best candidates. ZMR recrystallization material should be considered if simulations show that 0.25μm thick layers can be used.
3. For smart power applications, porous silicon or wafer bonding appear to be the best candidates.

The following is a summary of the main subjects presented during the meeting. A booklet containing 3-page extended abstracts of all contributions can be obtained from the editors, D. Bensahel and G. Bomchil, CNET/CNS, B.P. 98, Meylan 38243, France.

ZMR Techniques

The tendency is to recrystallize polysilicon layers on silicon dioxide using lamps or strip heaters in plain wafers, but this kind of recrystallization generally results in monocrystalline silicon with residual defects. Many efforts were dedicated to reducing this defect density. Present values are about 10^4 - 10^5/cm^2, and the defects are mainly threading dislocations. On the other hand it is possible to obtain perfect monocrystalline silicon if the localization of defects in pre-affected regions is accepted. Excellent results have been shown with structures presenting localization bands 4μm wide and perfect bands 36μm wide. In both approaches, however, thickness fluctuations of the silicon film on the order of 50 nm subsist. Two companies, Kopin in the United States and Micropolish in France produce SOI wafers using the ZMR technique.

Several papers discussed laser recrystallization for fabricating 3D structures. At present it is possible to recrystallize several levels. The best results for a mezzanine structure have been obtained using a selective epitaxial growth of silicon on the seed window before polysilicon deposition. For laser scanning it appears that the elliptical spots slanted from the scan direction give the best results. For multilevel structures the yield and quality of the recrystallized upper layer are very much degraded.

Electrical Measurements and Technology

It has been shown that technological processes are much easier on SOI materials than in bulk. This seems especially important for submicron technologies using very thin SOI films. Self-aligned very shallow junctions can be obtained without major precautions to prevent junction spikes. Many different devices have been fabricated in thin SOI layers and their performances compared with the equivalent bulk devices using the same technology. There is certainly an important speed gain. In fact the world speed record in silicon, 10 ps/gate, was obtained with ring oscillators in very thin SOI SIMOX material.

Water Bonding

While water bonding appears promising, some problems remain concerning the thinning of the wafer after bonding and defects at the outer borders of the bond region.

Porous Silicon

The physical phenomena of the mechanism of porous silicon formation are beginning to be studied in detail. As-formed porous silicon is saturated with Si-H bonds, and this seems to be the basis for many of the material's interesting properties.

On the technological side the n/n + /n structure has been proved to be very promising for obtaining SOI structures. Insulated layers as thin as 0.1 micron have been obtained and the electrical characteristics of the devices fabricated were very good. The electrical performance of transistors and ring oscillators in fully depleted layers without any kink effect are similar to the best results obtained in SIMOX materials. In addition, the porous silicon route appears to be of great interest for smart power applications because the oxide thickness can be increased up to 2-3 microns and the substrate quality is not degraded during formation and oxidation of the material.

SIMOX

Several papers showed how to decrease the dislocation density after oxygen implantation and annealing. An important paper drew attention to the properties of the oxide itself. It appears that under certain conditions the breakdown voltage of the oxide is low, on the order of 4-6 MV/cm. However, the material seems good because using appropriate annealing techniques overcomes most problems. Nearly no details were given about the implanting machine. □

See p. 44 in this issue for a description of upcoming workshops and schools in Europe.

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