

GFIS in Semiconductor Applications

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Electron beam and ion beam based techniques such as SEM, TEM, and FIB are used extensively by the semiconductor industry to provide analytical, metrology, and debug capabilities for process development, manufacturing yield monitoring, and new product ramp. The unique imaging and nanomachining attributes of the helium and neon Gas Field Ionization Source (GFIS) technology may extend beyond what electron and gallium beams can achieve alone. In this paper we will review key operating parameters, limitations, and novel application examples of the neon and helium beams for semiconductor applications.

It is well known that the ion beam resolution and probe current distribution strongly depend on the ion beam energy.¹ In the case of the gas field ionization source, these attributes also depend on the extraction voltage at the source region due to the ionization process.² For neon operation in particular, the trade-offs of the source extraction voltage and the beam acceleration voltage vs. the source stability and the emission current need to be taken.

Ion beam range and beam induced damage to active transistor devices and interconnect layers should be carefully minimized during GFIS imaging and nanomachining applications through beam energy and dose reduction. An invasiveness study on a seven stage ring oscillator in a 22 nm device quantified the beam induced damages to adjacent devices from both the neon and the gallium beams at various beam energies (Fig. 1). With the neon beam placed 15 nm away from the transistors, the oscillator timing degraded by 0.5% in the case of exposure from a 10 keV. The timing degradation of the oscillators from both 15 keV neon beam and 40 keV gallium beam exposure were at 1.5%. These results indicate that the neon beam can be safely used up to 15 keV without imposing worse timing invasiveness comparing to the current gallium techniques. This result has good agreement with the TRIM³ ion range simulation.

An application example of neon performing isolation cuts in TEM lamella is shown in Fig. 2. In this test case, a 15 keV neon beam was used to create a narrow isolation cut between adjacent contacts in a TEM lamella, which was extracted from a 14 nm process wafer. Encouraging results are demonstrated with a 14 nm wide cut achieved at the narrowest point of the separation and a 27 to 1 aspect ratio through the 380 nm thick membrane. Closer inspection reveals that the neon cut through the lamella is quite anisotropic with very little lateral damage to the adjacent process fins. Similar attempts to perform isolation cuts with Ga⁺ FIB showed that the Ga⁺ milling precision was ~2x greater in width; had a higher lateral defect density; and caused undesired metallic implantation to the test area, which could potentially convolute the result interpretation.

Additional helium and neon GFIS applications in fault isolation, failure analysis, and circuit edit will be discussed in this paper. Depending on applications, certain trade-offs of the imaging and nanomachining parameters needs to be made to enable successful implementation.

References:

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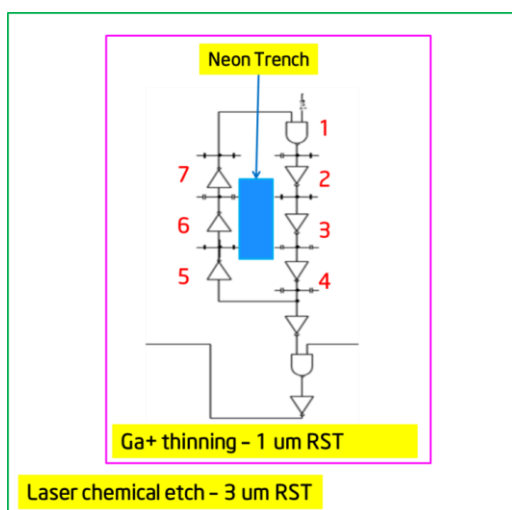


Fig 1. Graphical illustrations of the test area ring oscillator circuit and deprocessing steps used for the neon nanomachining timing invasiveness study.

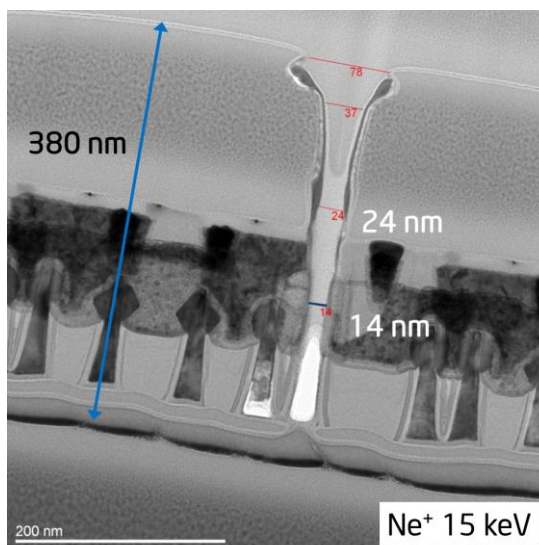


Fig 2. An example fault isolation cut in a TEM lamella using a 15 keV neon beam.