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Microscopy of Interconnects for 90nm Technology

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As IC devices become smaller and faster, the interconnects that connect the devices have scaled proportionately so that our newest 90nm technology has 90nm wide wires. Simultaneously the number of stacked metal layers has increased to seven and RC delay can limit performance. To minimize line resistance, the industry has moved from sputter-deposited aluminum to dual damascene electroplated copper lines and vias, surrounded by 3-10nm thick barriers, smoothed by chemical mechanical polish (CMP), and hermetically sealed. To minimize capacitance, SiO_2 has been replaced with carbon-doped oxide (CDO). The combination of Cu interconnects with CDO shows a 70% reduction in RC delay over aluminum with fluorinated SiO_2 [1]. However, the mechanical strength of the CDO film is significantly reduced and the stoichiometry and bonding in the CDO film depends upon processing conditions. As the device, interconnect, and chip size have fallen, the wafer size has increased, so that 90nm technology is produced on 300mm wafers. Each cm^2-sized chip can have roughly 1-1.5 *kilometers* of wire, which must be flawless.

The development challenge is to engineer each interface for performance, yield and reliability. Microscopists bring a suite of tools to apply to these challenges. Our challenge is to provide the fastest, most effective problem-solving techniques for characterization of good and bad interconnections, to match the electrical properties to the corresponding materials properties, and to correlate the materials properties to specific process steps.

Copper grain growth is determined by the phase of the barrier, the cleanliness of the seed surface, the line-width, the additives in the electroplating bath, deposition rate, the time between electroplating and chemical-mechanical polishing processing steps[2], as well as the obvious back-end thermal budget. We will show the results of several studies correlating copper microstructure to processing steps and yield.

Finding the weakest link in the 1 km of metal layers is a fault isolation and sample preparation challenge. Particles and voids are still yield killers. New defects to the Cu-low k system include Cu agglomeration because of poor wetting on barrier surface, Cu shorting because of its high ductility, poor adhesion and subsequent delamination, Cu corrosion, Cu out-diffusion through the barriers and barrier leakage. We will discuss location, characterization and prevention for these yield killers.

[1] S. Thompson et al. IEDM Tech. Dig. (2002)
[2] C. Lingk, M.E. Gross, W.L. Brown Appl. Phys. Lett. 74 682-684.

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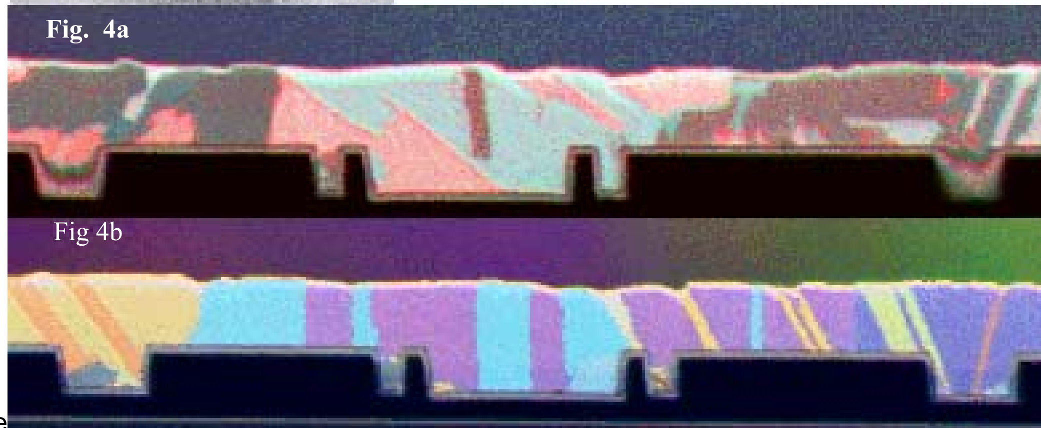
Fig. 1. Copper grains are columnar in the horizontal interconnects; smaller grains in the narrow vertical interconnect.

Fig. 2. A 2-nm break in the barrier caused failure of this vertical interconnect.

Fig. 3 Copper out-diffusion shows catastrophic barrier failure.

Fig. 4 Ion channeling images provide a snapshot of the grain structure a)with self anneal only – Cu grain growth occurs at room temperature and b)after 2 hour furnace anneal. Grain growth initiates at the free surface and extends into the patterned lines. Narrow lines have smaller grains than wide lines even after significant thermal treatment. The bulk copper will be removed by CMP to isolate the interconnects.



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