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Q.U.A.I.N.T.P.E.A.X. QUantifying Algorithmically INTrinsic Properties of Electronic Assemblies via X-ray CT

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Electronic assemblies such as printed circuit boards (PCBs) and integrated circuits (ICs) require precise fabrication and process control of the electrical and mechanical properties. Microelectronic fabrication is a combination of additive methods, such as deposition of metal layers [18]; or subtractive, such as etching or milling [19]. This stack of layers in PCB or IC design creates the connectivity required for each device to operate functionally within a range of design specifications such as electrical resistance or impedance. The non-destructive verification of final assembled devices has become widespread with access to high-energy metrology equipment, demand for trusted devices [13], and to mitigate the complex defect-prone multilayer designs in PCB (>8 Layer Lay-up) and IC (2.5D & 3D). Volumetric tools such as X-ray Micro Computed Tomography CT and Nano CT [9] are used to analyze the internal features of PCBs [5] and ICs [10] non-destructively. The automated quantification of these internal structures requires high-resolution data to provide enough spatial resolution throughout the sample's "sliced" volume. Each slice's resolution in the volume represents the spatial resolution of the X-ray scan collection. To quantify internal structures such as signal traces or via connections the internal feature must be processed to separate or segment individual components enabling automated dimensional analysis or material property characterization. As the miniaturization of device geometries and the density of components increases, the labor resources required for manual segmentation of layered volumetric data becomes impossible.

Small deviations in the mechanical lay-up of PCBs and ICs result in large changes in the electrical properties resulting in a percentage of yield for high volume production. Dielectric breakdown, electrical short circuit, and impedance mismatch are defects that can cause device failure [16]. These failures can be a product of manufacturing error or malicious alterations [6, 17], but research has shown that it can be prevented through physical inspection using X-ray CT to perform dimensional analysis [17].

This dimensional analysis can be performed algorithmically based upon image processing techniques such as template matching between similar layers in the volume to segment the device's layer stack-up. This template matching is combined with peak analysis to automatically quantify the layer information from a sample into 3D features, red X's represent regions where similarity based on intensity has significantly changed shown in Figure 1. These grouped 3D volumetric features can then be quantified analytically to determine their electrical properties such as impedance [12] for PCBs or connection density [3] in ICs. In the case where the spatial resolution of the X-ray scan is greater than the smallest internal features, these regions can be identified based on their attenuation or noise. For samples with regions of high attenuation and noise, the entire object can be analyzed via various sized kernels to determine the strongest contrast between layers; creating visual heatmaps of layered regions with strong correlation (blue) compared against poor layer matching (red) shown in Figure 2.

Automated volumetric layer analysis provides a high-throughput method of quantifying material properties such as dielectric constant, coefficient of thermal expansion [1], and corrosion [4] amongst large amounts of X-ray sample data without human intervention. This is accomplished through algorithmic dimensional analysis and conversion of its 3D structure to its material property characterization. Metrology performed upon the complex structure of electronic assemblies results in large

amounts of sample data [15]. This data can be analyzed automatically as opposed to manual inspection, and can be used for device lifecycle prediction [14], monitoring the effects of environmental stressors (e.g., temperature and humidity), and final assembly verification and/or assurance. Quantifying the intrinsic properties of a PCB or IC non-destructively via high throughput X-ray CT can be used to verify if a device's performance will operate safely in its designed environment. Devices including maliciously recycled, counterfeit, or out-of-spec samples [8] can be identified based upon their altered material properties such as warpage [2], composition [20], etc. While external analysis via optical tools can provide a level of verification, internal micro and nanoscale analysis is necessary to verify an entire device's functionality or to perform failure analysis.

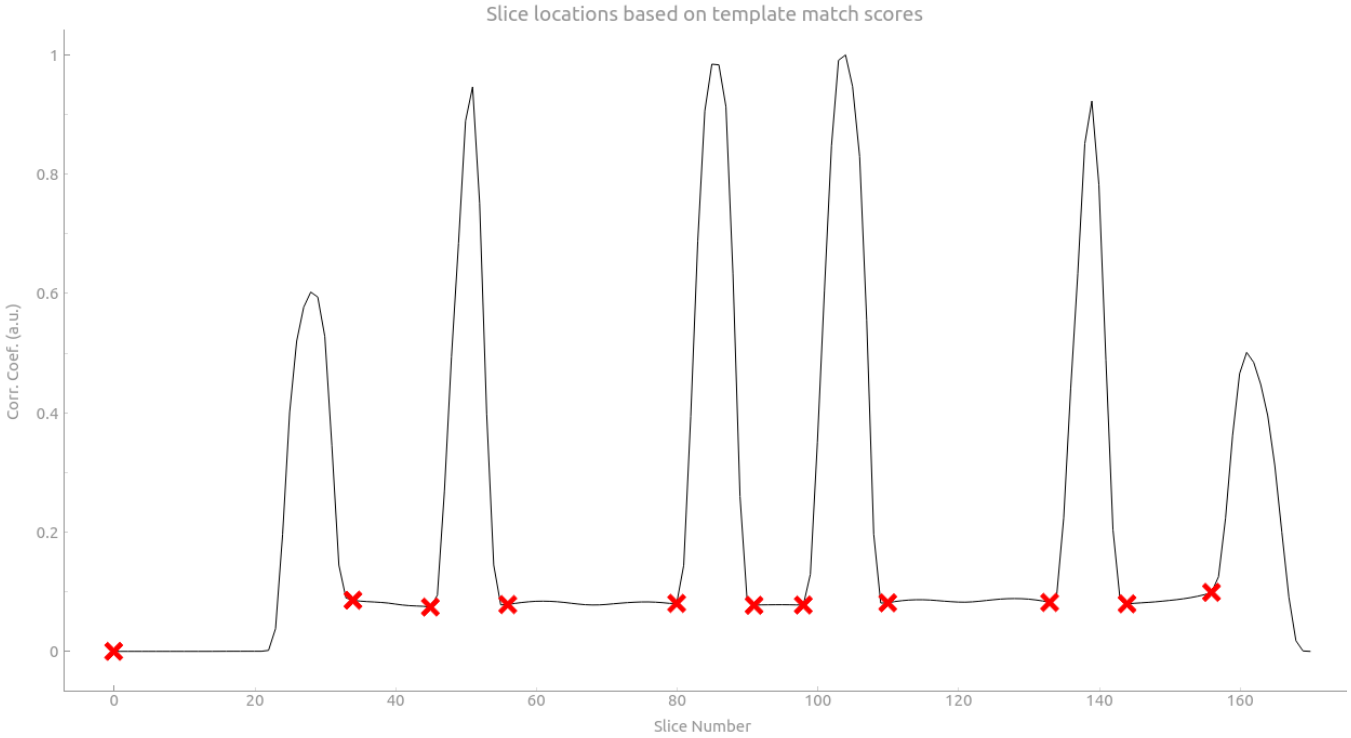

Figure 1. Figure 1: Peak Analysis Graph representing template matching scores on the Y-axis indicating "sliced" regions of similar pixel intensity values where the X-axis represents the numbered "slices" of pixels from inside the 3D volume. Red X's represent slices where pixel similarly has significantly changed from the previous slice, resulting in segmented regions in-between these changing regions. Higher intensity peak values result from layers with more "on" (white) pixels throughout the image compared to the "off" pixels of the background, such as the case for via layers, where the amount of "on" pixels is limited.

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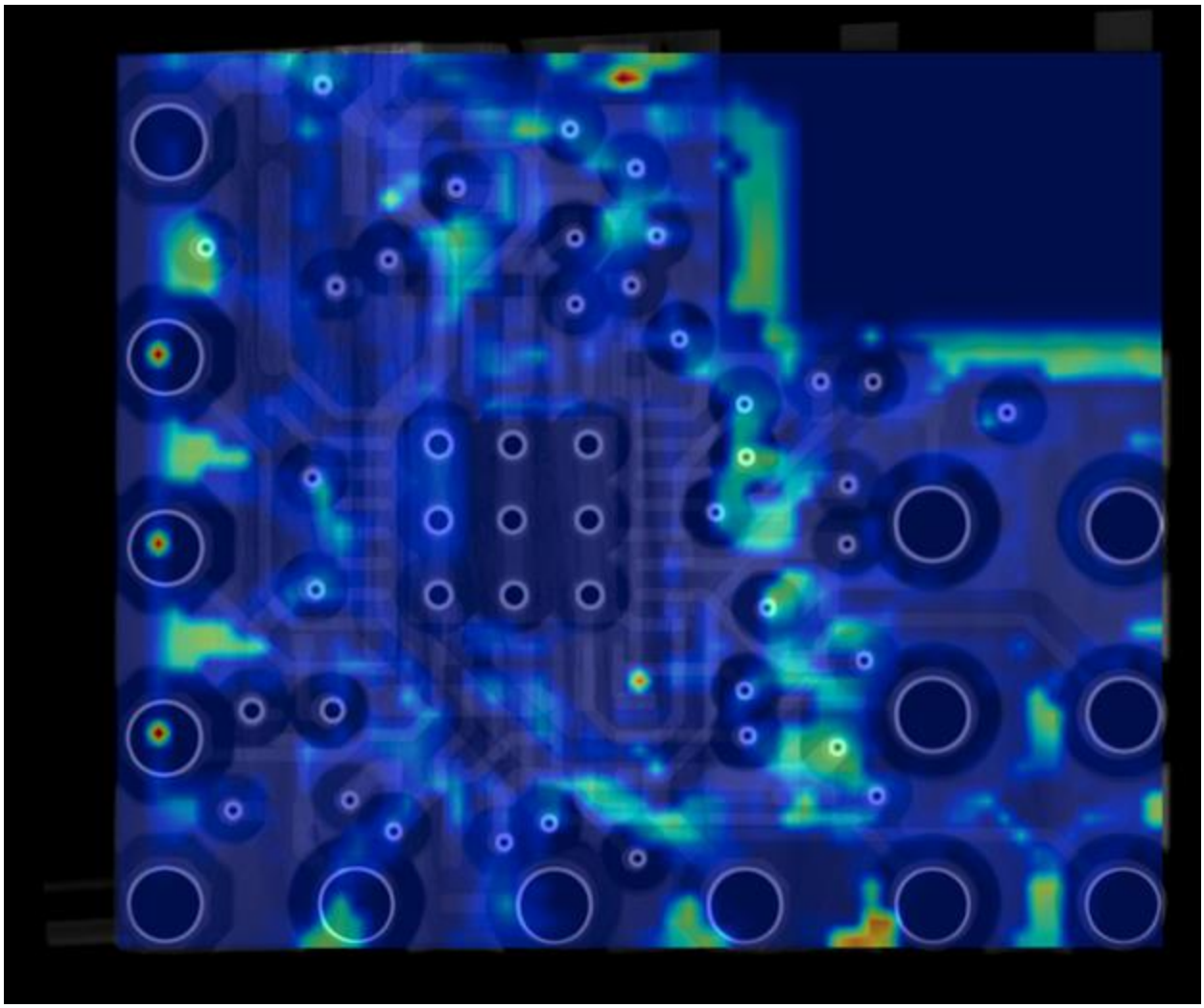

Figure 2. Figure 2: Heatmap of multi-layer (6 Layer) printed circuit board; hot spots denotes the kernel region of strongest peak metrics where layers appear distinct within a small window. Red regions indicate highly distinguishable regions where automated segmentation has determined the strongest metric values.

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